Intel's 65 nm Logic Technology Demonstrated on 0.57 μm^2 SRAM Cells

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What are We Announcing?

- Intel has fabricated fully-functional 4 Mb SRAM arrays using an ultra-small 0.57 μm^2 SRAM cell on its 65 nm generation logic technology
- The 65 nm process incorporates key technology elements needed on high performance microprocessors, including strained silicon transistors and 8 layers of copper interconnect using a low-k dielectric
- Intel's advanced in-house mask making capabilities allow us to extend 193 nm lithography tools down to the dimensions needed on the 65 nm generation
- The 65 nm logic technology is being developed in Intel's newest 300 mm fab, D1D, in Hillsboro, Oregon

Why is this Important?

- Demonstrates that Intel continues to track Moore's Law, delivering a new process technology every 2 years
- Demonstrates the value of in-house mask making capabilities to enable continued dimensional scaling while using cost effective lithography tools
- Demonstrates the advantage of an Integrated Device Manufacturer: Ability to control all the critical pieces (silicon process, mask making, circuit design) and control the increasingly complex interactions between them

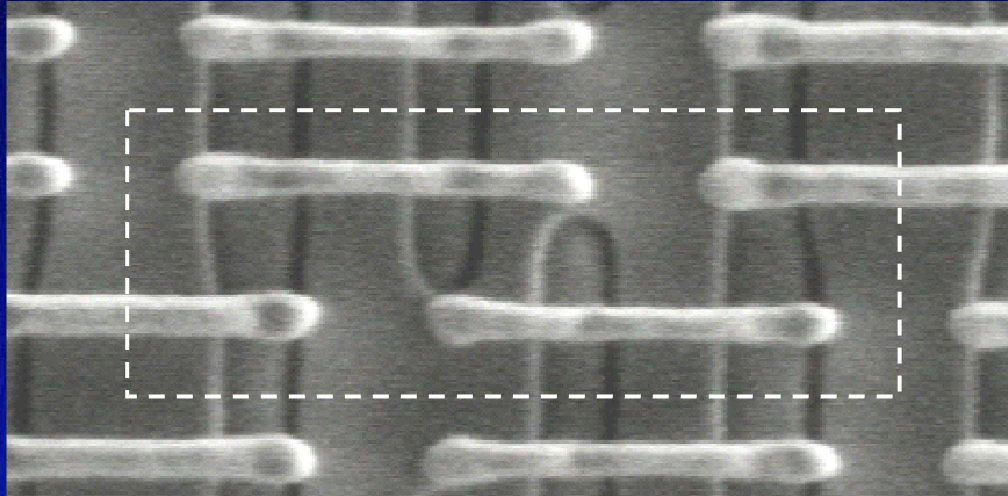
Intel's Logic Technology Evolution

Process Name	P858	Px60	P1262	P1264	P1266	P1268
1st Production	1999	2001	2003	2005	2007	2009
Lithography	0.18µm	0.13µm	90nm	65nm	45nm	32nm
Gate Length	0.13µm	0.70µm	50nm	35nm	25nm	17nm
Wafer (mm)	200	200/300	300	300	300	300

Moore's Law continues!

Intel continues to introduce a new technology generation every 2 years

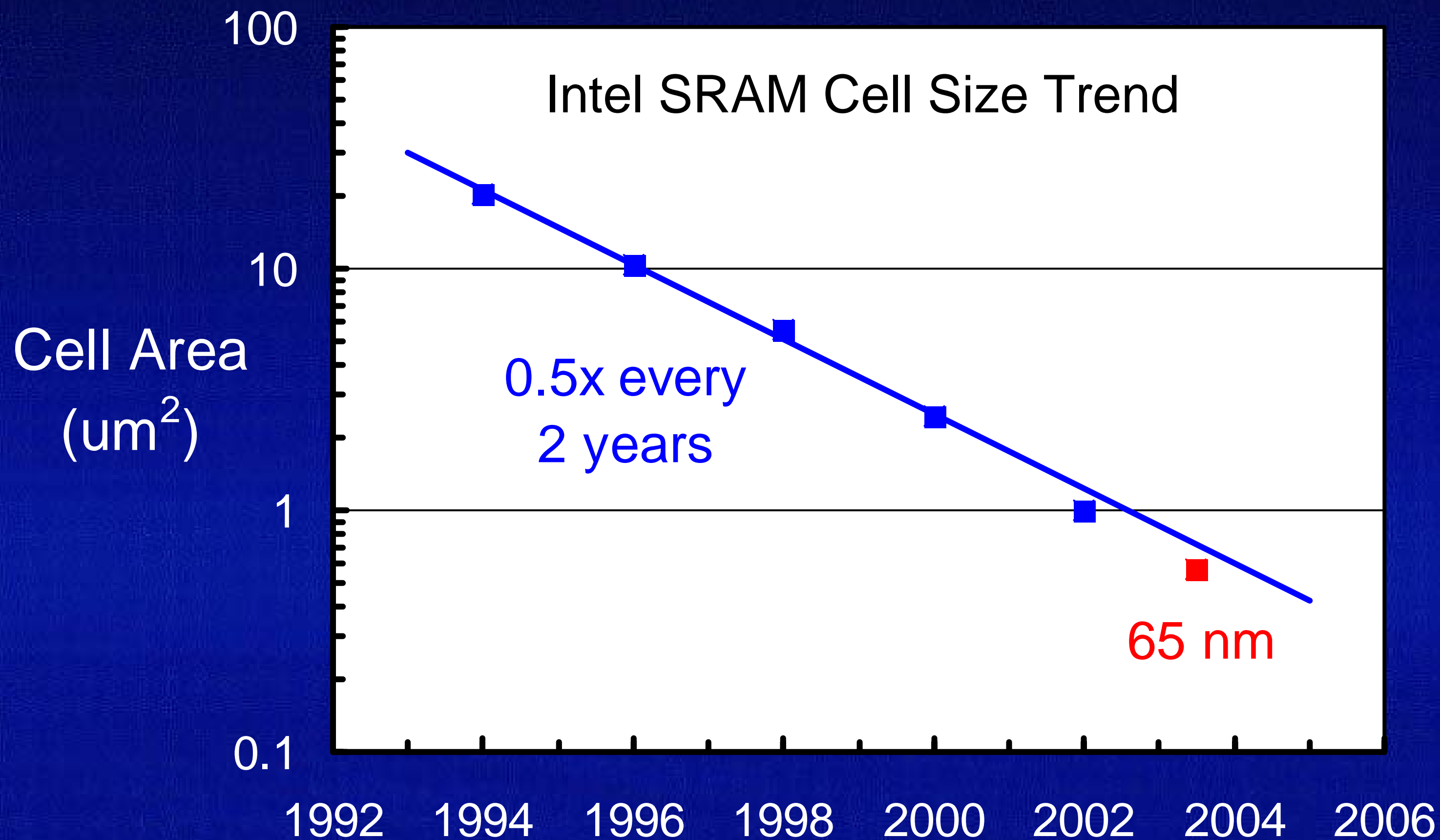
0.57 μm^2 6-T SRAM Cell



0.46 x 1.24
= 0.57 μm^2

- Ultra-small SRAM cell used in 65 nm process packs six transistors in an area of 0.57 μm^2
- Fully functional 4 Mbit SRAM arrays have been made with all bits working
- Approximately 10 million transistors could fit in the area of the tip of a ball point pen (1 mm^2)

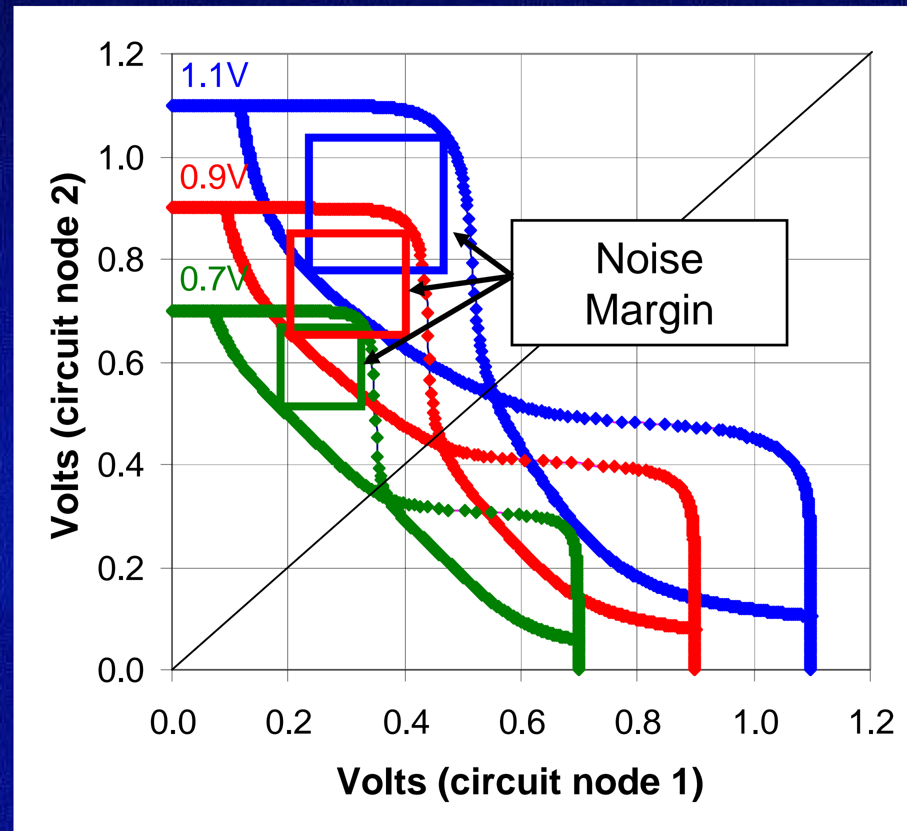
Doubling Transistor Density Every 2 Years



0.57 μm² cell on 65 nm process was demonstrated only 20 months after 1.0 μm² cell on 90 nm process

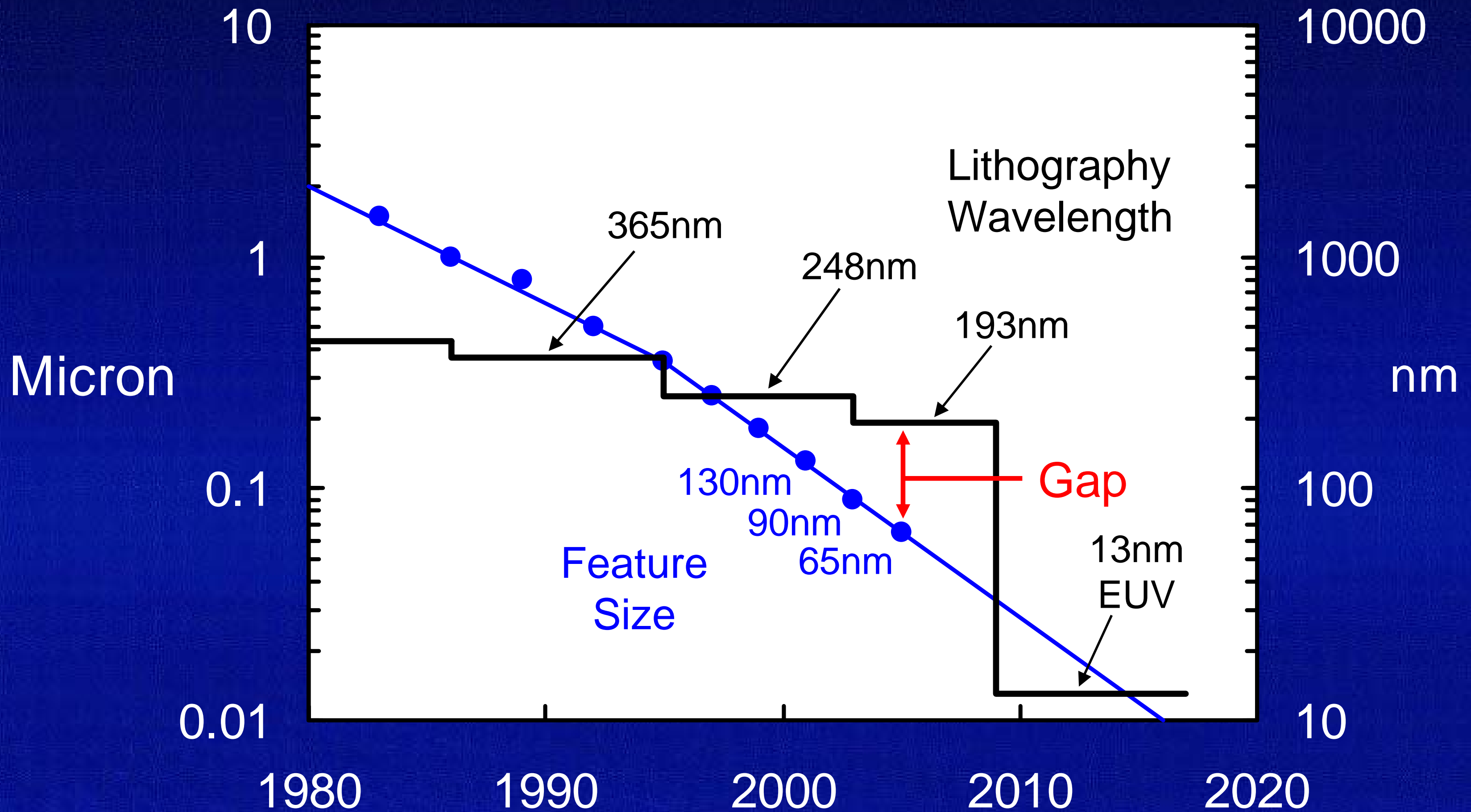
SRAM Noise Margin

- Small area is not the only important factor for SRAM cells
- Adequate noise margin for robust circuit operation is critical, and can be hard to achieve at small dimensions and low voltages
- Intel's 0.57 μm^2 SRAM cell has solid noise margin even down to a 0.7V operating voltage



Measured internal voltage levels on 0.57 μm^2 SRAM cell

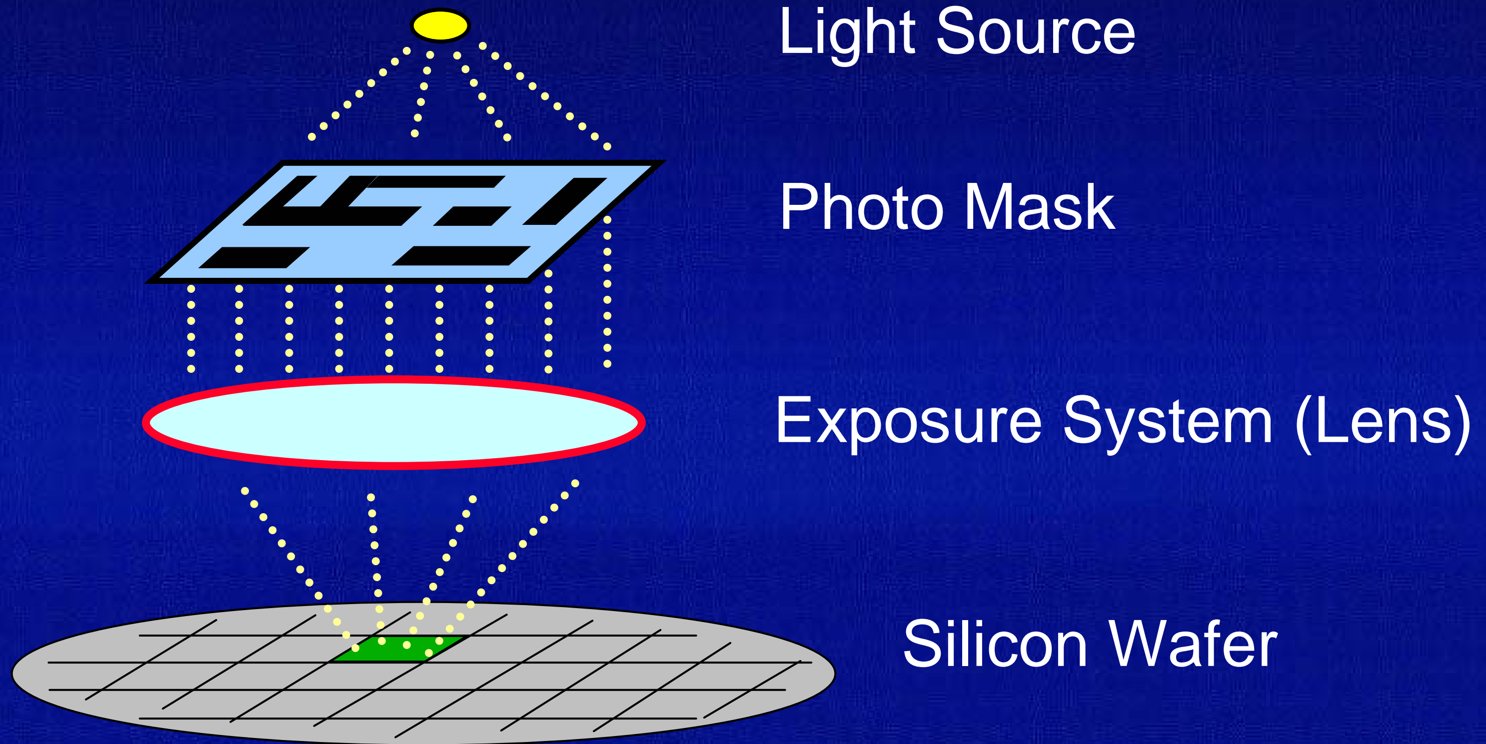
Lithography Challenge



Minimum feature size is scaling faster than lithography wavelength

Advanced photo mask techniques help to bridge the gap

How are Photo Masks Used?



In-House Mask Facility

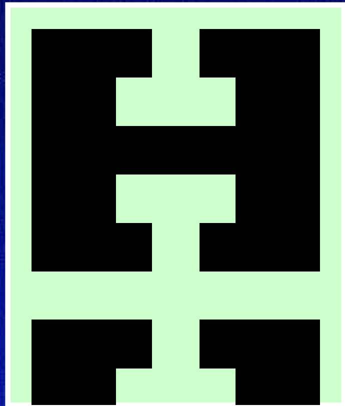
Intel's in-house mask making facility was critical to achieving this 65 nm SRAM cell milestone

In-house mask facility:

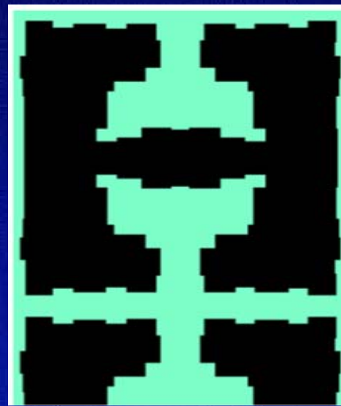
- State-of-art 35k sq ft clean room
- Providing all Intel mask needs including the management of ~15% outsource for back-up purposes
- Fast delivery (5 days for 1ST 3 layers)
- Lowest return rate in the industry
- Advanced OPC and phase shift masks for 65 nm node
- World leading EUV mask development program for possible 32 nm node insertion

OPC Masks

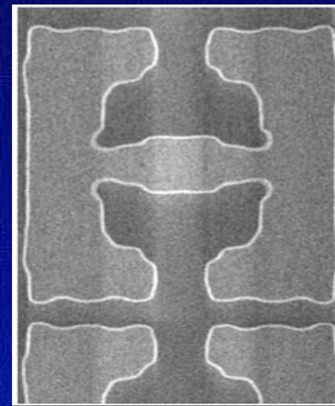
Top View



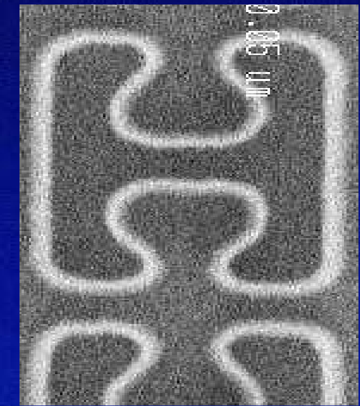
Drawn structure



Add OPC features



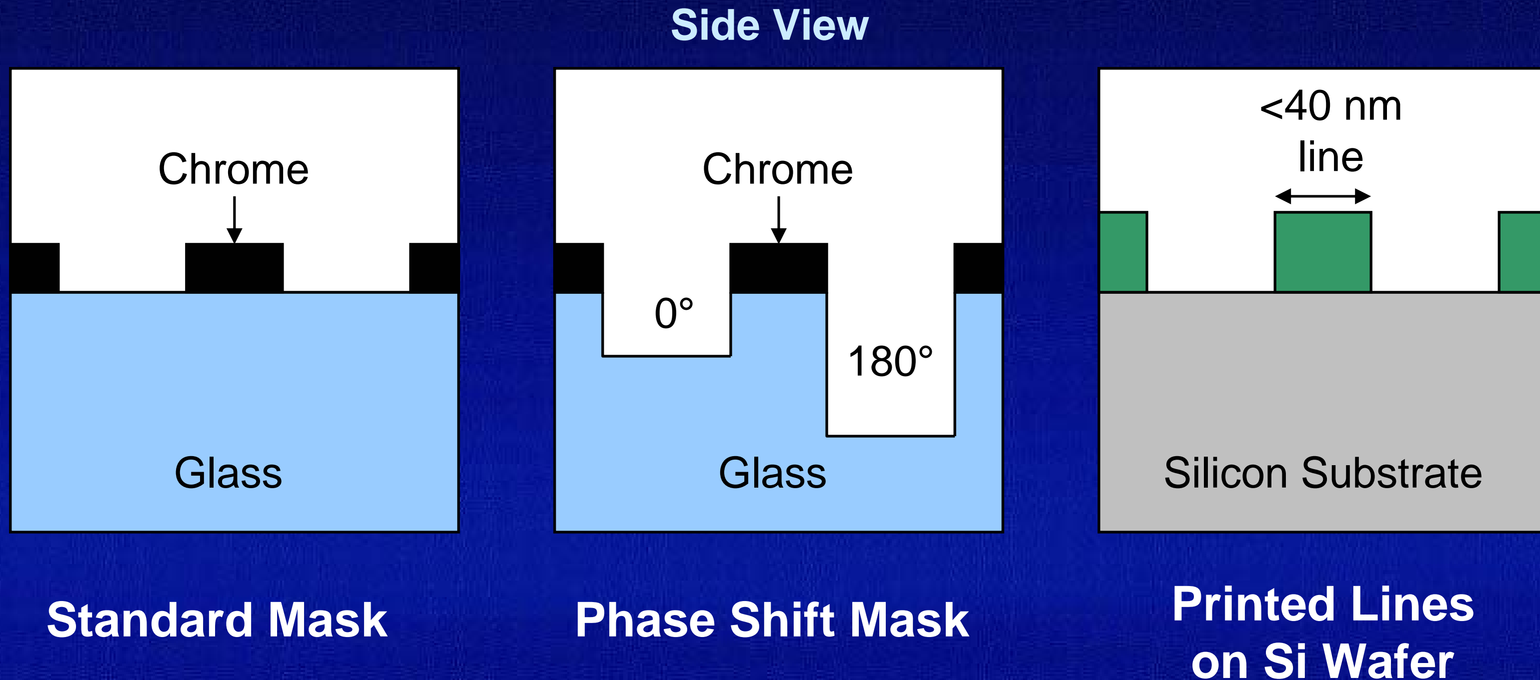
Mask structure



Printed on wafer

- Sub-resolution Optical Proximity Correction features added during mask making to enable improved pattern definition
- OPC requires sophisticated algorithms for adding sub-resolution features and requires improved mask making technology

Alternating Phase Shift Masks



- Phase shift masks enable patterning <40 nm lines using 193 nm wavelength light
- APSM requires both new mask making technology and new circuit layout design rules

D1D - World's Most Advanced Fab

- Intel's 65 nm logic technology is being developed at our 300 mm wafer fab, D1D, located in Hillsboro, Oregon
- D1D is Intel's newest fab and is our 4TH operational 300 mm facility
- At 176,000 sq feet, D1D is Intel's largest individual clean room (roughly the size of 3.5 football fields)
- Fully automated wafer transport is used to move 300 mm wafers throughout the fab
- D1D will be used to both develop and manufacture Intel's 65 nm and 45 nm logic technologies

65 nm Wafer Fab – D1D

Hillsboro, Oregon

World's most advanced 300 mm wafer fab

Summary

- Intel has demonstrated fully functional 4 Mb SRAM arrays with a cell size of only 0.57 μm^2 using our 65 nm logic technology
- The process flow used incorporates key elements needed for advanced microprocessors, such as strained silicon transistors and 8 layers of Cu interconnects using a low-k dielectric
- Intel's advanced in-house mask making capability is instrumental in extending 193 nm lithography tools to the 65 nm generation
- The 65 nm logic technology is being developed in the world's most advanced 300 mm fab, D1D, in Hillsboro, Oregon
- Intel is on track for being the first to produce 65 nm generation microprocessor products in 2005

For further information on Intel's silicon technology,

please visit the Silicon Showcase at

www.intel.com/research/silicon