90 nm Generation, 300mm Wafer Low k ILD/Cu Interconnect Technology

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ABSTRACT

This paper presents a 90 nm generation and 300 mm wafer size interconnect technology with 7 layers of Cu metallization and low k ILD. Carbon doped oxide (CDO) low k ILD is used to achieve > 20% inter- and intra-layer capacitance improvement and 25-30% RC improvement over 130 nm generation SiOF interconnect process with equivalent electro-migration performance.

INTRODUCTION

As the logic design rules scale down to below 130 nm, backend interconnect RC delay becomes critical to overall chip performance and power consumption. High performance, high yield and low cost Cu metallization were successfully introduced in the earlier generations [1,2] to reduce the metal line resistance, R. Advanced low k ILD (intrinsic k <3) is the key focus of 90 nm node[3] interconnect integration to improve the capacitance part of the time delay.

However, all low k ILD materials exhibit much weaker mechanical strength in every category, including modulus, hardness, adhesion and cohesive strength, than SiOF and oxides used in the previous generations. The developmental work done to overcome the challenges and to integrate low k ILD with Cu in order to achieve the desired RC delay improvement, yielding, and reliability performance is presented in this paper.

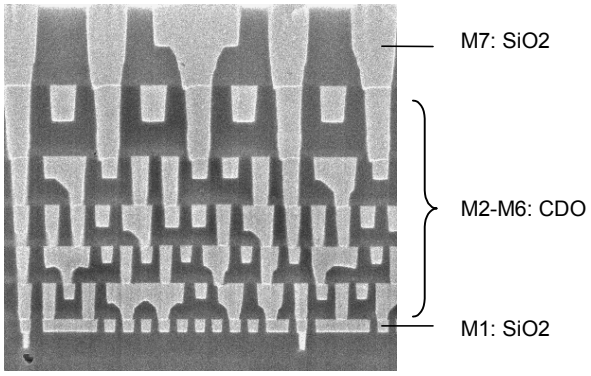

Fig. 1. Cross-sectional SEM photograph showing 7 Cu interconnect layers with either CDO or SiO2 dielectrics.

PROCESS FEATURES AND PERFORMANCE

Materials and Integration Schemes

This interconnect technology features seven layers of Cu metallization/low k ILD to boost up interconnect performance over 130 nm technology as (Fig. 1). Progressive metal pitches are used for density and yield consideration with a minimum pitch of 220 nm at the metal 1 layer to over one micron at the metal 7 layer as shown in Table 1. Via first dual damascene integration scheme is used for process simplicity and better design rule control. A simple single ILD/ Etch-stop stack is deployed on all layers for cost efficiency and better capacitance performance as shown in Fig. 2. Note that M1 and M7 ILD stacks each are SiO2/SiN and the rest are CDO Low k ILD stacks.

Metal Layers	Pitches	Metal Line AR	Metal Thickness
M1	220 nm	1.4	150 nm
M2	320 nm	1.6	256 nm
M3	320 nm	1.6	256 nm
M4	400 nm	1.6	320 nm
M5	480 nm	1.6	384 nm
M6	720 nm	1.6	576 nm
M7	1080 nm	1.8	972 nm

Table 1. Summary table for pitches, AR and metal thickness for this technology.

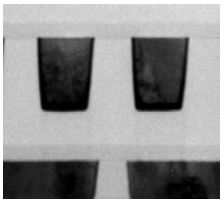

Fig. 2. A TEM image showing simple single ILD/Etch-stop layer stack.

The low k ILD material that has been chosen for Intel 90 nm interconnect technology is Carbon-Doped Oxide (CDO). All CDO materials exhibit degraded mechanical properties and adhesion performance compared to the Fluorine-doped oxide (SiOF/FSG) used in 130 nm technology. Fig. 3 shows the trade-offs between hardness, one of the key mechanical properties, and the intrinsic dielectric constant, k, of various ILD materials, including CDO, SiOF, oxides and spin-on polymer (SOP). CDO films with an intrinsic k of < 3 is best for the balance between performance and sufficient mechanical strengths for packaging and reliability.

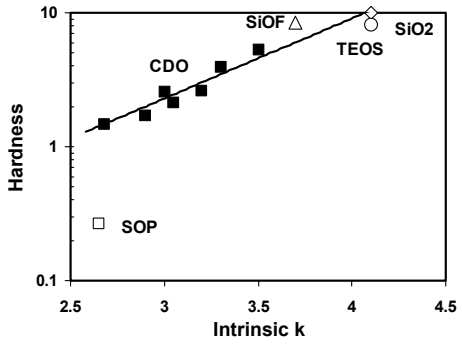

Fig. 3. Hardness vs. intrinsic dielectric constants benchmark for various types of ILD materials.

The primary roles of the oxide layers at M1 and M7 are to enhance the mechanical strengths of the entire interconnect stacks. The top oxide layer can shield mechanical and thermal stress that occurs during assembly and packaging. Secondly, the compressive stress of oxide layers serves as a clamp to balance the high tensile stress of CDO films. As shown in Fig. 4, the stress at the end of the line is close to neutral with compressive oxide layers at the top. The overall ILD stack reliability is greatly improved.

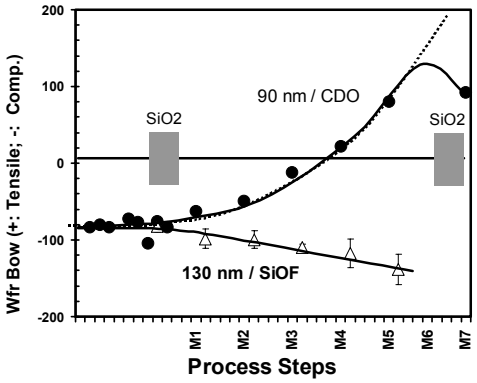

Fig. 4. Wafer level stress as a function of process steps for 90 nm CDO technology and 130 nm SiOF technology. Note that the tensile stress development in CDO stacks is offset by the compressive stress of the oxide layer at the top.

Performance-Vias

With the technology scaling, via resistance increases dramatically due to scaled via CD. The via resistance can limit the interconnect performance and yield if not controlled. In the dual damascene process, the via resistance is mainly determined by the barrier materials and via bottom barrier thickness, which is limited by the minimum sidewall barrier coverage.

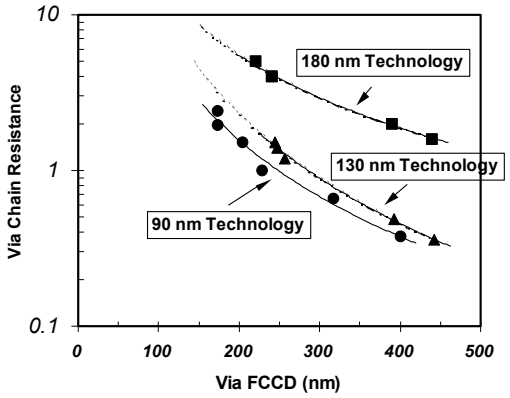

Fig. 5. Normalized via chain resistances as a function of via CDs of various process technologies.

A conformal barrier deposition technique, such as ALD (Atomic Layer Deposition), yields minimum via bottom barrier thickness. However, most of the ALD materials that have been developed so far exhibit high resistivities and hence no advantage in the (resistivity*via bottom barrier thickness) metrics. An improved conventional barrier deposition process has been developed in this process technology to improve the sidewall barrier coverage and to allow a reduction of via bottom barrier thickness and via resistance as shown in Fig. 5.

Performance-Metal Lines

The metal line resistance in general is impacted by the aspect ratio (AR), barrier thickness, Cu grain boundary pinning/grain size and sidewall scattering effect. Fig. 6 shows a sharp increase of metal line resistance when the metal line CD is below 150 nm. Cu grain size engineering and process improvements in reducing metal line roughness, and sidewall barrier coverage are crucial for meeting resistance performance goals.

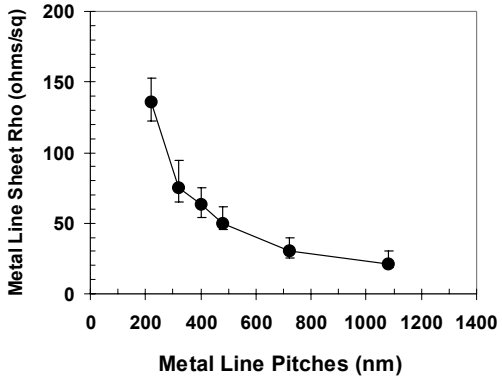

Fig. 6. Metal line sheet rho as a function of metal line pitches. Note the sharp increase when metal line CD below 150 nm.

Performance-Capacitance

The line-to-line capacitance of this process technology has been improved by 22% over the 130nm node by using CDO low k ILD as shown in Fig. 7. The overall RC improvement is over 30% for the 130 nm technology node from the combination of low k ILD and the improved Cu metallization process (Fig. 8).

To achieve capacitance performance for low k ILD, one of the biggest challenges is to prevent process damage either from plasma processing or wet cleans to CDO. Novel process improvements to limit the plasma damages and wet clean effects are critical to achieve maximum and consistent capacitance improvement from low k materials.

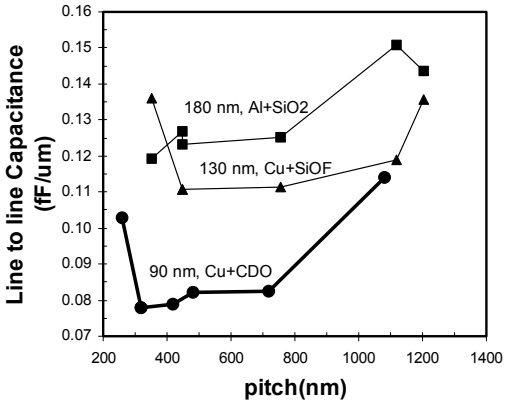

Fig. 7. Line to line capacitance as a function of metal line pitches. 90 nm CDO exhibits 20-25% of capacitance improvement over 130 nm SiOF technology.

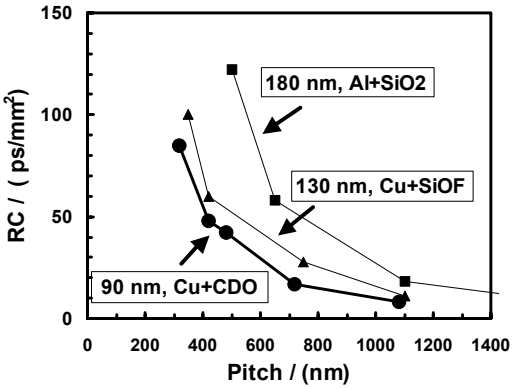

Fig. 8. RC performance trending of 180nm, 130 nm and 90 nm interconnect technology as a function of metal line pitches.

Reliability/EM

Figure 9 shows the historical trend of Cu/low k electro-migration time to failure distributions. The first data on Cu integrated with low k materials was severely impacted by the assembly process used for the test units. This process caused a breach in the passivation layers leading to a loss of hermeticity that severely degraded the parts performance. After the assembly process was improved, approximately a 10x degradation in electro-migration performance with the low k materials was still observed. To fix this, process improvements were pursued that did not involve a change to the intrinsic low k materials. By optimizing Cu and etch-stop layers deposition conditions lifetimes better than SiO_2 based units were achieved.

300mm Wafer Size Scaling

This interconnect technology has been demonstrated on 300 mm wafers using 52 Mbits SRAM test chips with 1 um^2 6-T cells. Fully functional chips are being routinely made without incorporating redundancy. There are more than 100 billions of transistors and contacts and more than 30 billion of vias in a single wafer. Figs. 10 show a single SRAM chip and a 300 mm wafer fabricated with this interconnect process, respectively. The biggest challenges of 300mm wafer scaling are uniformity control and mechanical damages to the wafers.

CONCLUSIONS

A 90 nm generation interconnect technology has been developed on 300 mm wafers with seven layers of advanced Cu metallization and CDO low k ILD. Excellent interconnect performance, yields and reliability are demonstrated with 52 Mbits SRAM chips.

REFERENCES

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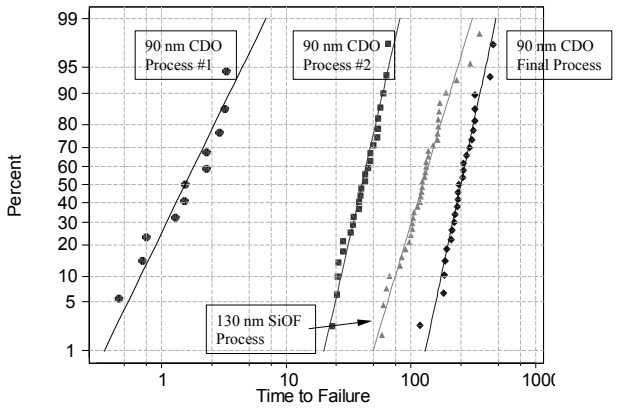
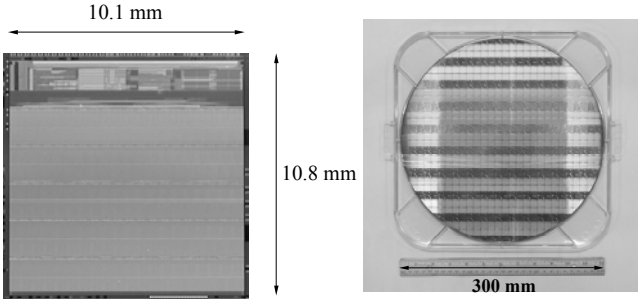


Fig. 9. Electro-migration performance trending of low k ILD development.



Figs. 10. (left) A single 52 Mbits SRAM chips with 9this technology. (right) A 90 nm technology generation 300 mm wafers with low k ILD and Cu interconnects.