Novel InSb-based Quantum Well Transistors for Ultra-High Speed, Low Power Logic Applications

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Outline

- Introduction
- InSb as High Mobility Channel Material
- InSb Materials Growth and Results
- InSb QW Transistor Fabrication
- Device Characterization and Results
- Benchmarking of InSb based Transistors to Silicon based Transistors for Logic Applications
- Conclusions

Channel Material Properties at 295K

	Si	GaAs	$In_{.53}Ga_{.47}As$	InAs	**InSb**
Electron Mobility ($cm^2V^{-1}s^{-1}$) $n_s=1x10^{12}/cm^2$)	600	4,600	7,800	20,000	**30,000**
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	**5.0**
Ballistic Mean Free Path (nm)	28	80	106	194	**226**
Energy Band-gap	1.12	1.42	0.72	0.36	**0.18**

- **InSb shows the highest room temperature mobility, but also the lowest energy band-gap**

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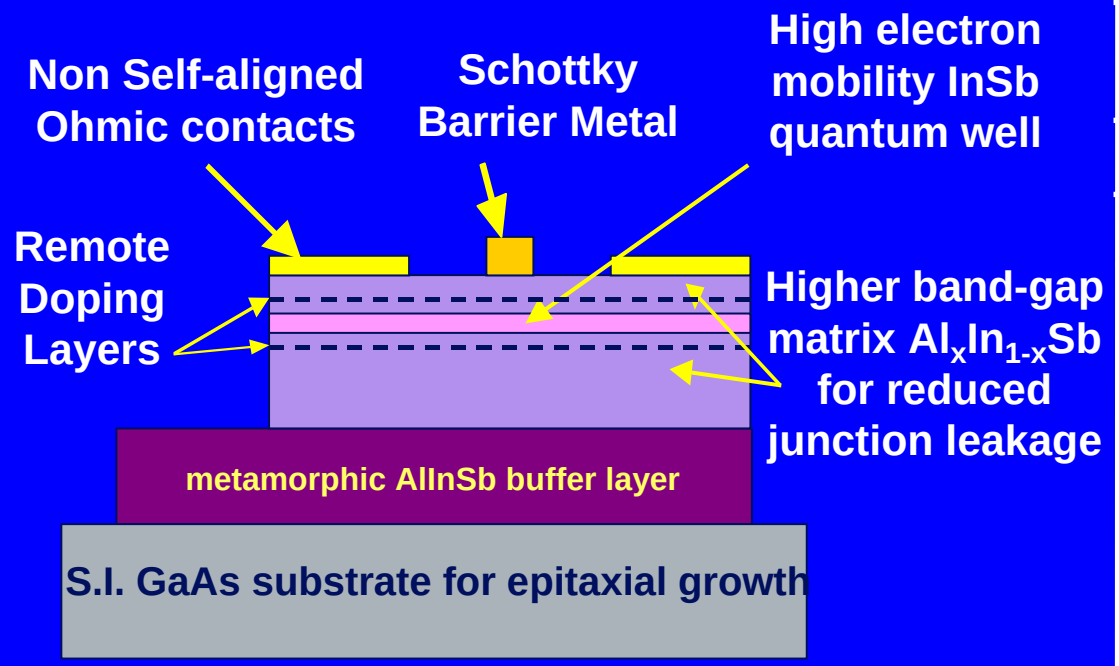
InSb Quantum Well Transistor and Multi-layer Epitaxial Structure



Layer	Material	Thickness (nm)
Top Barrier	$Al_xIn_{1-x}Sb$	15-45
Doping	Te	-
Spacer	$Al_xIn_{1-x}Sb$	5
Channel	InSb	20
Metamorphic Buffer	$Al_yIn_{1-y}Sb$	3,000
Substrate	GaAs	

- Carriers are confined within the InSb quantum well for transport
- InSb is embedded in a matrix of higher band-gap material, $Al_xIn_{1-x}Sb$, to reduce leakage

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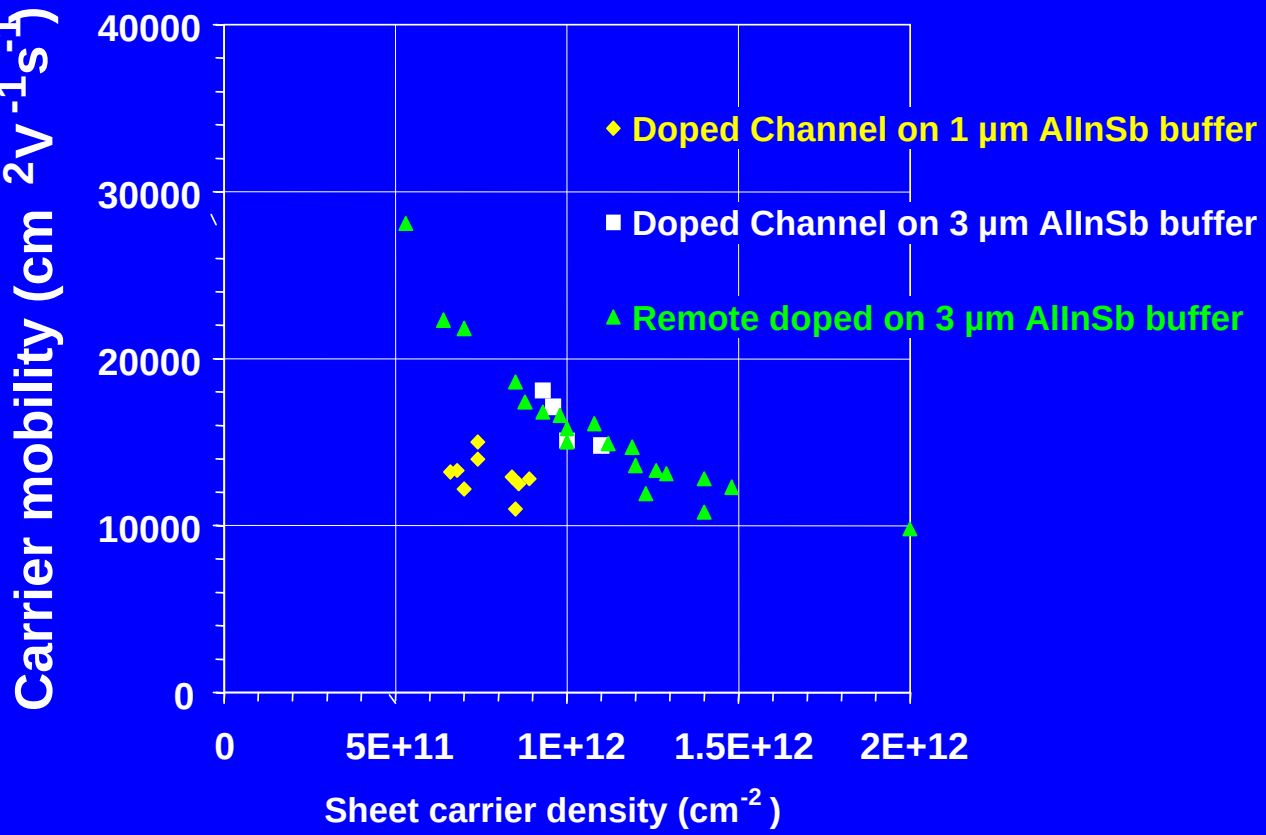
Hall Mobility of Doped versus Modulation Doped InSb Channel



- Thicker buffer layer improves InSb QW mobility
- Modulation doping with $Al_{.15}In_{.85}Sb$ barrier layer improves mobility only at low carrier densities.

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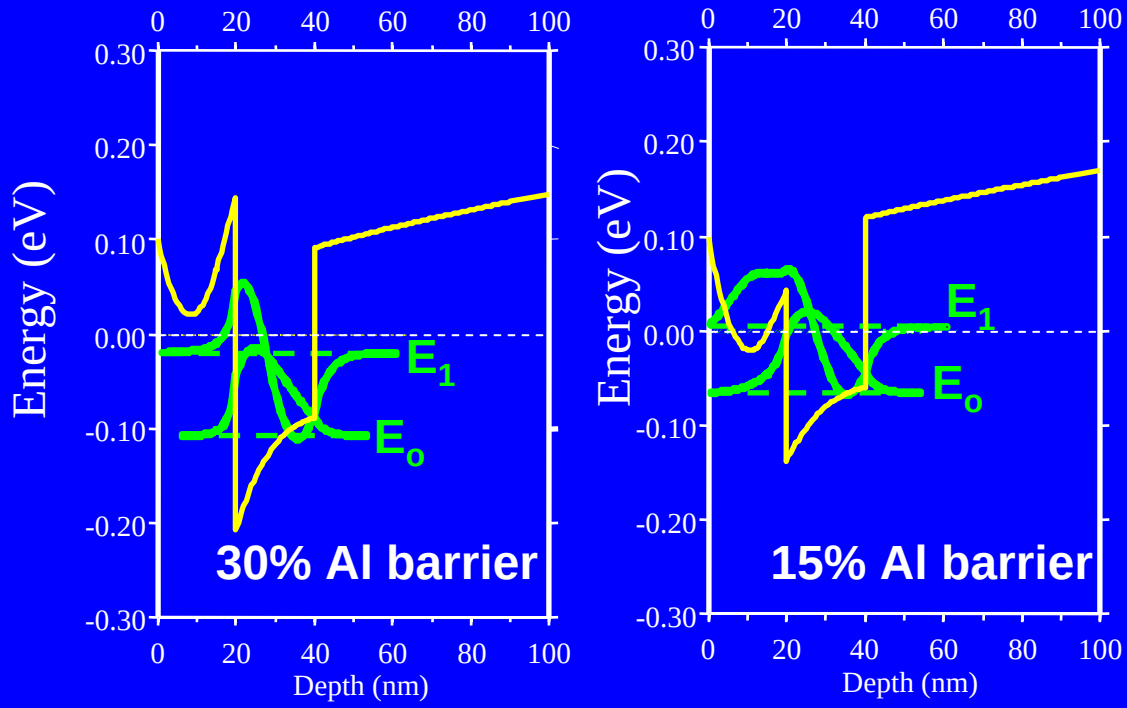
Schrödinger Poisson Simulation of Carrier Confinement in QW



- **Higher conduction band offset barrier results in increased confinement of electrons within the InSb QW at high carrier densities.**

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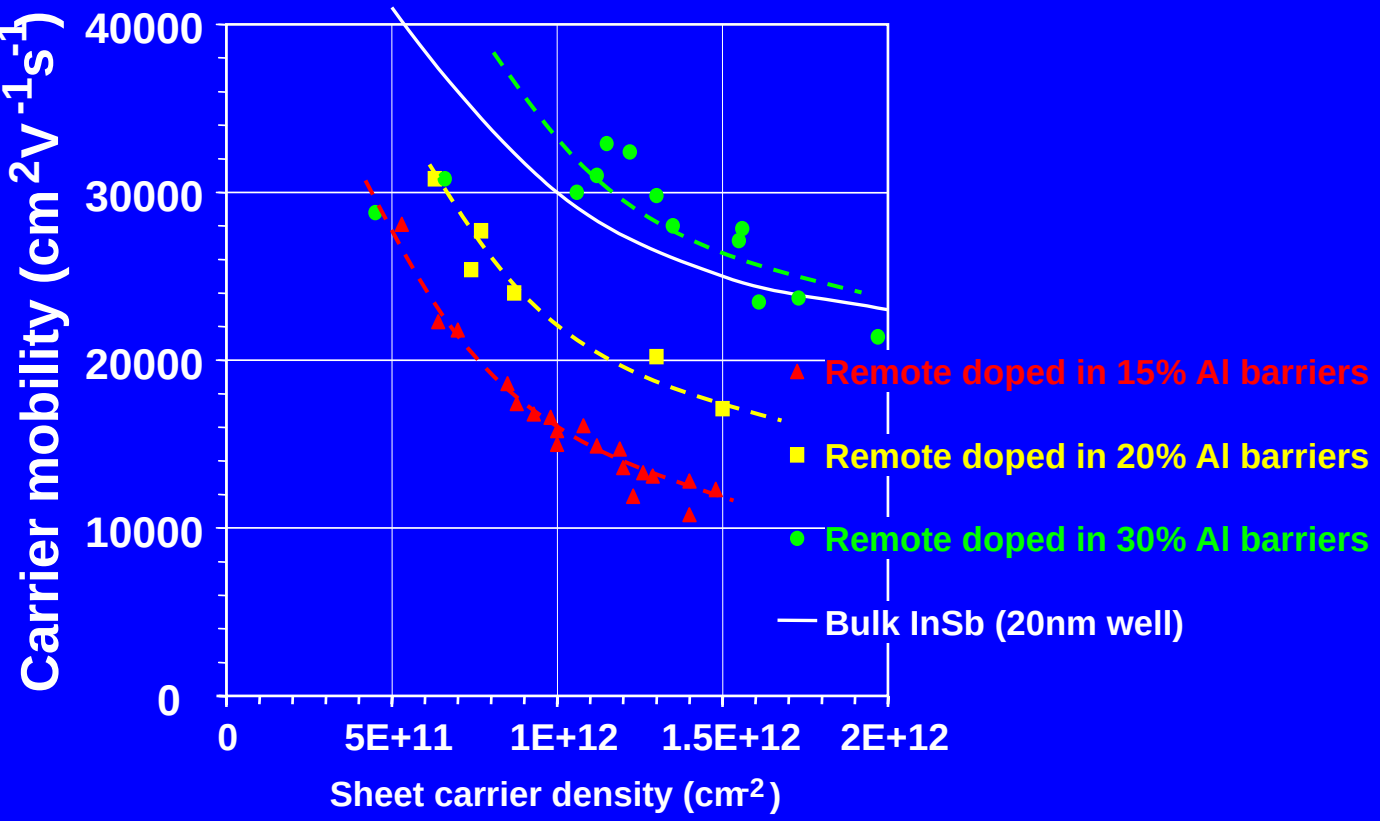
Hall Mobility of Modulation Doped InSb Quantum Well



- Room temperature InSb QW mobility over 30,000 $cm^2V^{-1}s^{-1}$ is achieved with 30% Al barrier at $n_s = 1.3\times10^{12}$ cm^{-2} !

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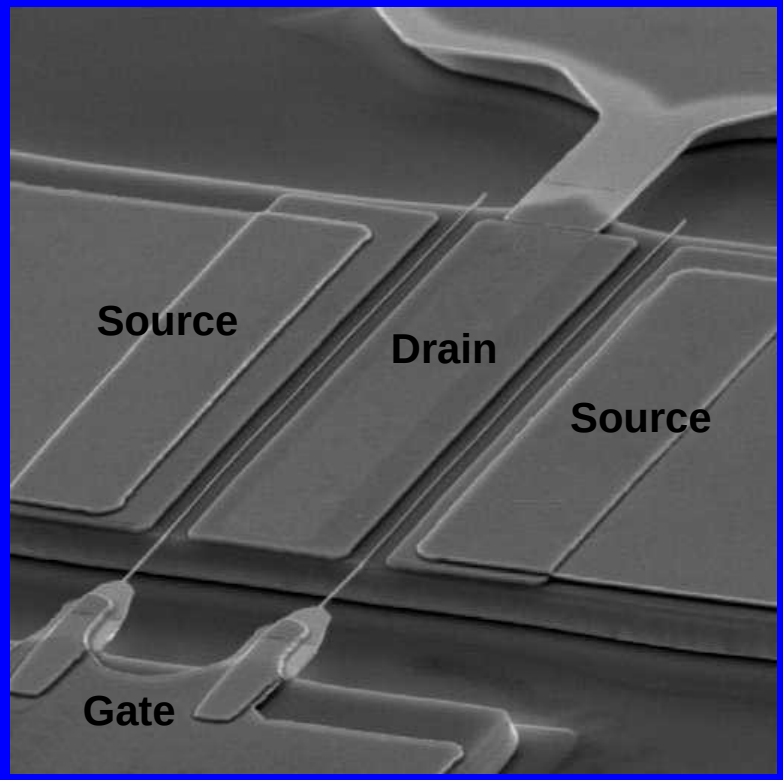
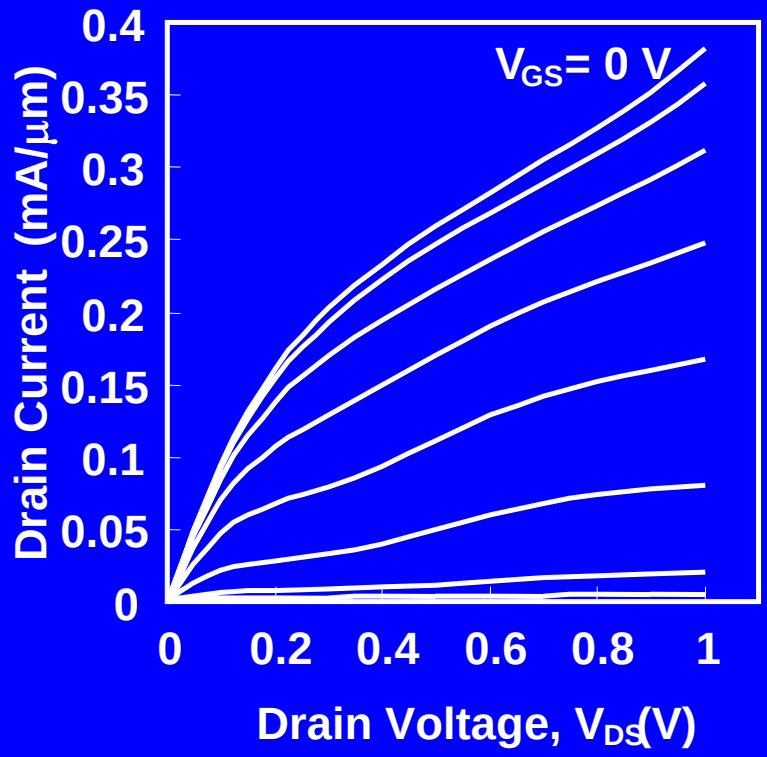
InSb QW Transistor Fabrication





- A two gate finger InSb QW transistor (LG=200nm) fabricated with gate air-bridge using mesa isolation
- DC output characteristics show breakdown voltage above 1.2V

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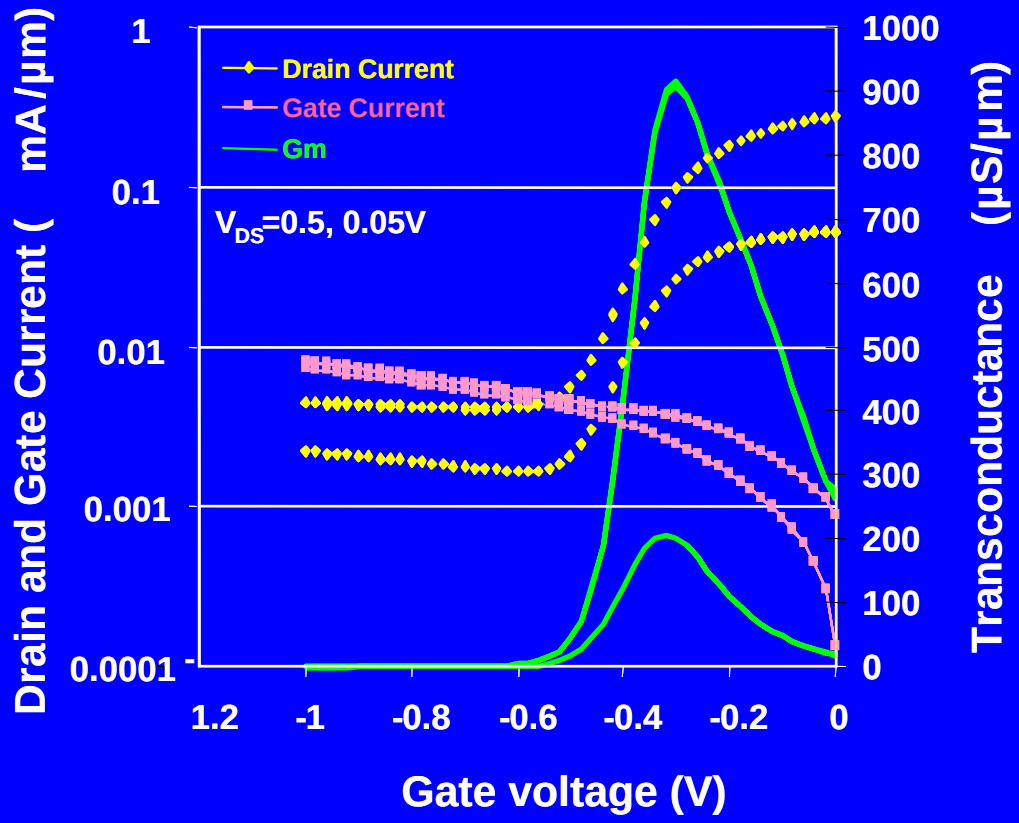
InSb QW Transistor DC Characteristics



- Peak gm of 900 μS/μm is obtained with 200nm L_G devices
- Schottky gate leakage limits the off-state leakage current

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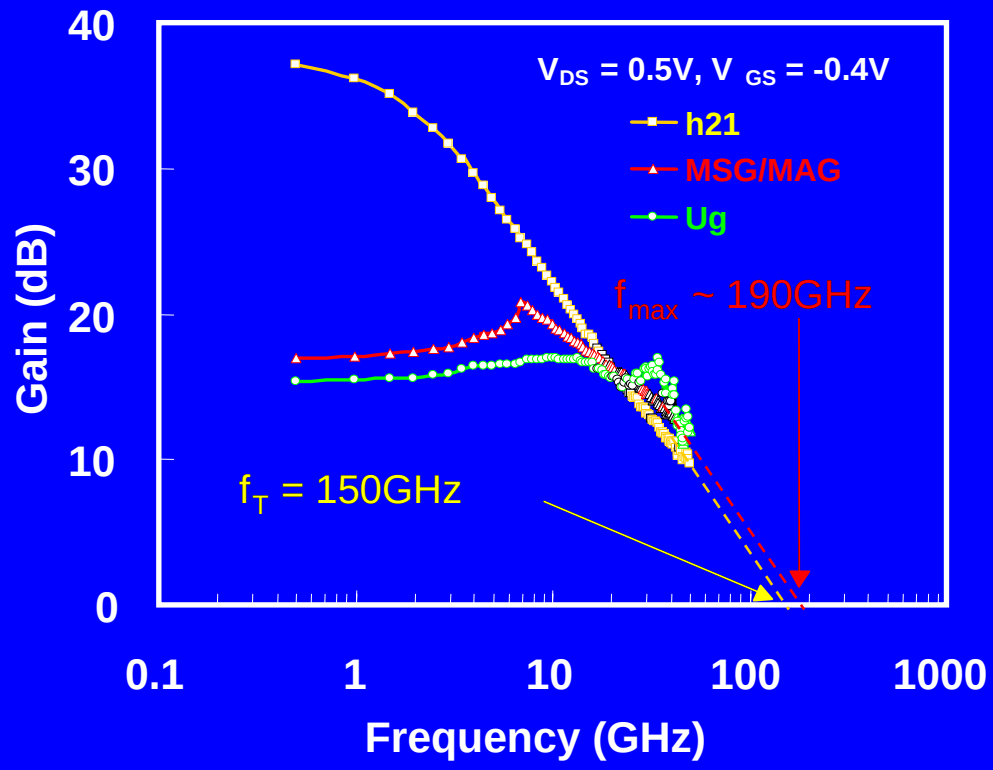
InSb QW Transistor High Frequency Characteristics



- Unity gain cut-off frequency, f_T ~ 150GHz is achieved with 200nm LG InSb QW transistor
- This corresponds to intrinsic gate delay (CV/I) of 1ps.

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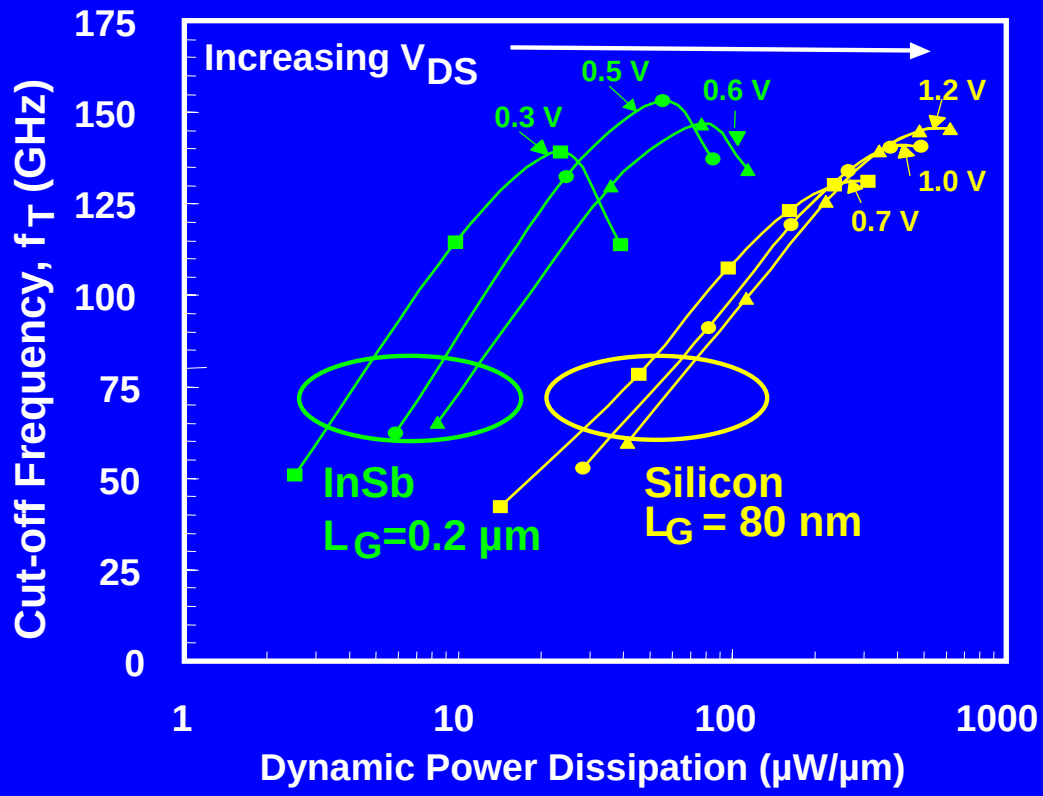
Performance and active Power Trade-off



- **InSb QW transistors provide equivalent high frequency performance as state-of-the-art Si transistors with 10X lower active power dissipation.**

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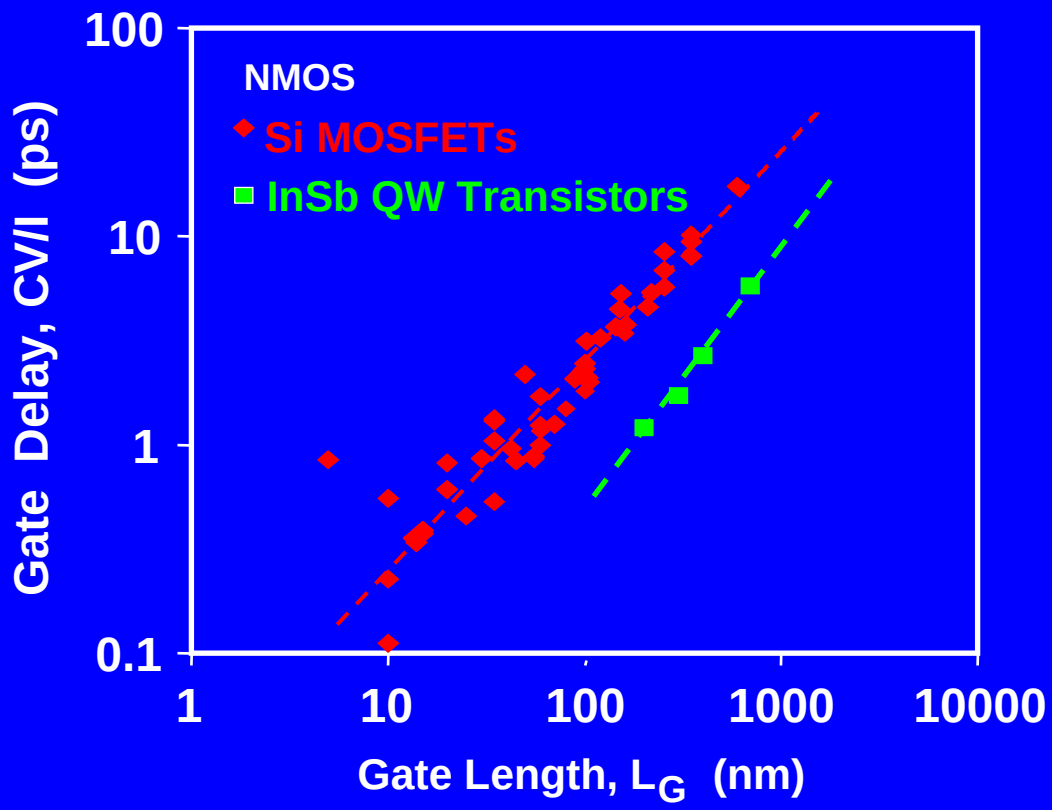
Gate Delay vs Gate Length



- InSb QW transistors provide 5X improvement in intrinsic gate delay over Si transistors at similar L_G
- Scalability of InSb QW transistors still remain to be demonstrated

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Conclusions

- Room temperature mobility of 30,000 $cm^2V^{-1}s^{-1}$ has been achieved with InSb quantum well.
- InSb QW transistors are demonstrated to operate in depletion mode at 0.5V V_{DS} (0.5V VGS swing), with an Ion-Ioff ratio ~ 80 and fT ~ 150 GHz
- InSb QW transistors (L_G = 200nm) show equivalent high frequency performance as Si transistors (L_G = 80nm) with 10X lower active power dissipation
- Schottky gate leakage sets the Ioff limit for the InSb QW transistors
- Future InSb-based transistors will require a) high-K dielectrics to reduce I_G and b) enhancement mode operation to reduce I_{OFF} for potential applications in ultra high speed, low power logic applications.

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