Novel InSb-based Quantum Well Transistors for Ultra-High Speed, Low Power Logic Applications

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Abstract

InSb-based quantum well field-effect transistors with gate length down to 0.2 µm are fabricated for the first time. Hall measurements show that room temperature electron mobilities over 30,000 $cm^2V^{-1}s^{-1}$ are achieved with a sheet carrier density over 1×10^{12} cm^{-2} in a modulation doped InSb quantum well with $Al_xIn_{1-x}Sb$ barrier layers. Devices with 0.2 µm gate length and 20% Al barrier exhibit DC transconductance of 625 µS/µm and f_T of 150 GHz at V_{DS} =0.5V. 0.2 µm devices fabricated on 30% Al barrier material show DC transconductance of 920 µS/µm at V_{DS} =0.5V. Benchmarking against state-of-the-art Si MOSFET's indicates that InSb QW transistors can achieve equivalent high speed performance with 5-10 times lower dynamic power dissipation and therefore are a promising device technology to complement scaled silicon-based devices for very low power, ultra-high speed logic applications.

1. Introduction

Indium antimonide (InSb) shows great promise as an ultra-fast, very low power digital logic technology as it has the highest electron mobility and saturation velocity of any known semiconductor (Table 1). This performance can be accessed at room temperature using Extractive™ (minority carrier exclusion and extraction) technology, which mitigates the effect of the narrow band-gap on device leakage and breakdown. This was earlier demonstrated in a MISFET device, using an InSb device layer on an InSb substrate with a deposited SiO_2 gate oxide [1]. In this paper, we report on the materials growth, device fabrication and characterization of an InSb channel quantum well FET, which uses a semi-insulating GaAs substrate, a relaxed metamorphic buffer layer of $Al_yIn_{1-y}Sb$ to accommodate lattice mismatch, a compressively strained InSb quantum well confined between layers of $Al_xIn_{1-x}Sb$ and a Schottky barrier metal gate. Careful materials structure design employing a modulation doping scheme achieves 295K electron mobility of over 30,000 $cm^2V^{-1}s^{-1}$ with a carrier density of over 1×10^{12} cm^{-2}. Devices with gate length of 0.2 µm are fabricated and characterized, which demonstrate an f_T of 150 GHz at V_{DS} = 0.5V. Benchmarking with state-of-the-art Si-based NMOS devices indicate that InSb-based transistors achieve equivalent high speed performance with 5-10 times lower DC power dissipation, with potential for further increasing the performance when scaled to state-of-the-art Si device gate lengths.

Table 1. Channel Material Properties at 295K

	Si	GaAs	$In_{.53}Ga_{.47}As$	InAs	InSb
Electron Mobility ($cm^2V^{-1}s^{-1}$ $n_s=1x10^{12}/cm^2$)	600	4,600	7,800	20,000	30,000
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	5.0
Ballistic Mean Free Path (nm)	28	80	106	194	226
Energy Band-gap	1.12	1.42	0.72	0.36	0.18

2. Materials Growth and Results

The InSb quantum well material was grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. The layers from bottom to top consist of an accommodation layer, a 3 µm $Al_yIn_{1-y}Sb$ buffer, a 20 nm thick InSb quantum well, a 5nm thick $Al_xIn_{1-x}Sb$ spacer, a Te δ-doped donor sheet (~1×10^{12} cm^{-2}) and a 15-45 nm thick $Al_xIn_{1-x}Sb$ barrier layer (Table 2). Hall measurement of mobilities was performed at room temperature. Structures with the quantum well doped directly n-type with Te impurities gave carrier densities (n_s) in the range of 0.8-1.2$\times10^{12}$ cm^{-2} and mobilities in the range of 14,000-18,000 $cm^2V^{-1}s^{-1}$. These were improved over earlier layers grown on 1 µm metamorphic buffer layers due to better material quality. We have also implemented a modulation doping scheme, with a Te δ-doped donor layer introduced in the

Table 2. Multi-Layer Structure for Device Fabrication

Layer	**Material**	**Thickness (nm)**
Top Barrier	$Al_xIn_{1-x}Sb$	15-45
Doping	Te	-
Spacer	$Al_xIn_{1-x}Sb$	5
Channel	InSb	20
Metamorphic Buffer	$Al_yIn_{1-y}Sb$	3,000
Substrate	GaAs	

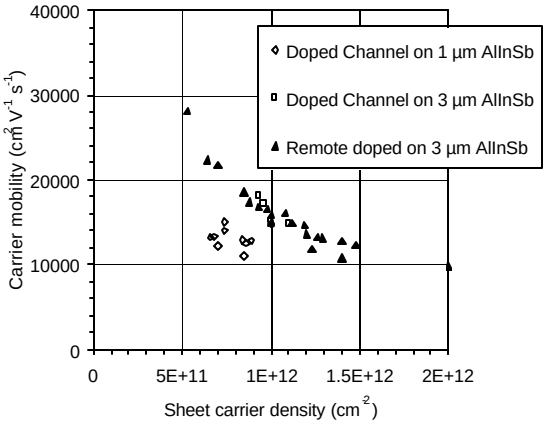

Figure 1. Hall Mobility data on directly doped and modulation doped 20nm thick InSb quantum wells with 15% Al in the $Al_xIn_{1-x}Sb$ barrier layer.

barrier layer above the quantum well, separated by a spacer layer. Single field Hall mobility measurements versus sheet carrier densities (n_s) are shown in Figure 1. Modulation doped structures achieve a very high electron mobility of 30,000 $cm^2V^{-1}s^{-1}$ with $n_s = 5\times10^{11}$ cm^{-2}, but drops to around the same mobility ~16,000 $cm^2V^{-1}s^{-1}$ as the directly doped structures for $n_s = 1\times10^{12}$ cm^{-2}. It is believed that, in this regime, the mobility is not limited by ionized impurity scattering, despite the drop in mobility versus carrier density, since both the modulation-doped and the direct-doped structures show very similar mobility at high carrier densities, and both are below the expected value from an equivalent bulk-doped layer. Self-consistent Schrödinger-Poisson modeling of carrier distributions show that at higher carrier densities more carriers start to populate higher energy sub-bands that spread into the barriers, with consequent lower mobility, as shown in Figure 2. This modeling also predicts that using higher conduction band offset barriers would give increased mobility. We have grown layers with increased Al percentage in the barriers that show, for a given carrier density, the quantum well mobility increases monotonically with increasing Al percentage from 15% to 30%. Hall mobility measurements show that, with 30% Al in the barrier layers, the quantum well mobility achieved is over 30,000 $cm^2V^{-1}s^{-1}$ at $n_s = 1.3\times10^{12}$ cm^{-2}, which is above the bulk InSb mobility versus doping concentration trend-line (Figure 3).

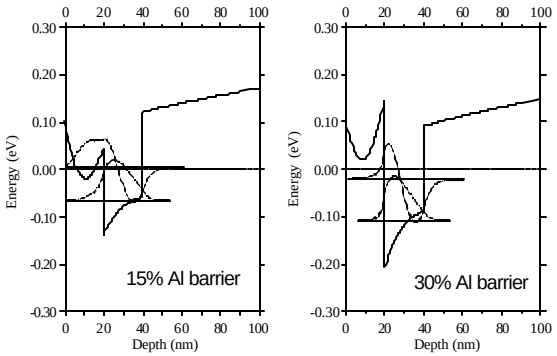

Figure 2. Calculated band structure and Schrödinger-Poisson solution of spatial redistribution of confined carrier population in various sub-bands in the quantum well for 15% and 30% Al percentage barriers.

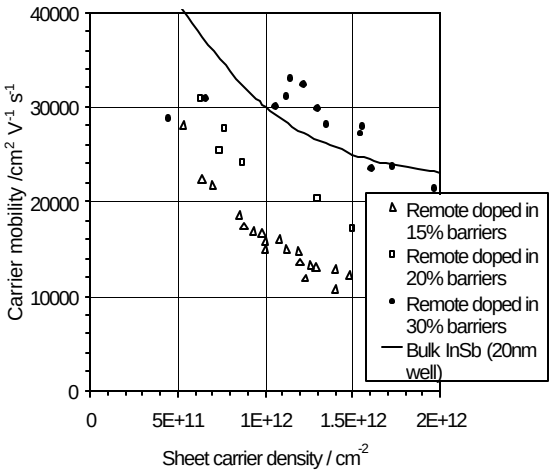

Figure 3. Hall Mobility data on modulation doped 20nm thick InSb quantum wells with 15%, 20% and 30% Al in the $Al_xIn_{1-x}Sb$ barrier layer.

3. Transistor Fabrication

Two types of multi-layer epitaxial structures were used in this work to fabricate devices down to 0.2 µm gate length. Type A material consists of a 20 nm modulation doped InSb quantum well with a 50 nm 20% Al barrier with an average mobility of 30,000 $cm^2V^{-1}s^{-1}$ at $n_s = 6.5\times10^{11}$ cm^{-2}. Type B material has a 20 nm 30% Al barrier with an average mobility of 32,000 $cm^2V^{-1}s^{-1}$ at $n_s = 1.3\times10^{12}$ cm^{-2}. First, in the fabrication process sequence, the source and drain ohmic contacts are defined using optical lithography. Ti/Au layers are then deposited by e-beam evaporation and lift-off. After the ohmic contact formation, the Ti/Au Schottky gate metallization is performed using e-beam lithography, e-beam evaporation and lift-off process. Finally, device isolation is achieved by wet chemical etching resulting in a gate air-bridge at the mesa edge between the channel and the gate feed metal (Figure 4).

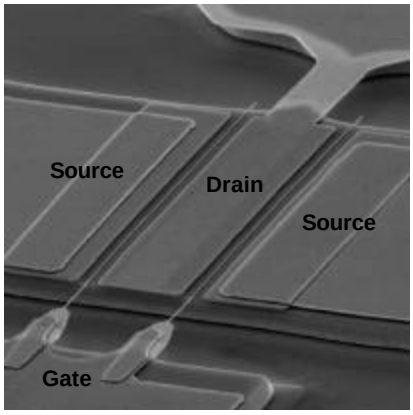

Figure 4. SEM micrograph of a two-finger InSb quantum well transistor with gate air-bridge at the mesa edge. L_G = 0.2 µm, L_{DS} = 2.0 µm.

4. DC Characterization

The InSb quantum well transistors were fabricated with gate lengths in the range 0.2-0.4 µm. A typical room temperature output characteristic of a 0.2 µm transistor fabricated on Type A material with a 50 nm 20% Al barrier is shown in Figure 5. The device exhibits good saturation characteristics with a knee voltage of 0.2 V and an off-state breakdown voltage of over 1.2 V. The low field source-drain resistance of this device is 1.2 Ω-mm, with source-drain separation of 2 µm and an ohmic contact resistance of 0.24 Ω-mm.

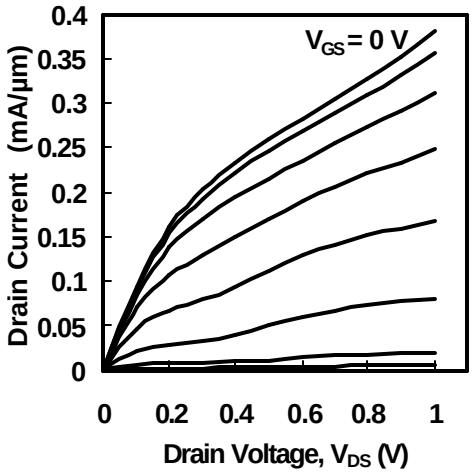

Figure 5. 0.2 µm L_G InSb QW transistor output characteristics at 295 K, Type A material, L_{DS} = 2 µm, W_G = 80 µm, V_{GS} = 0.1 V/step.

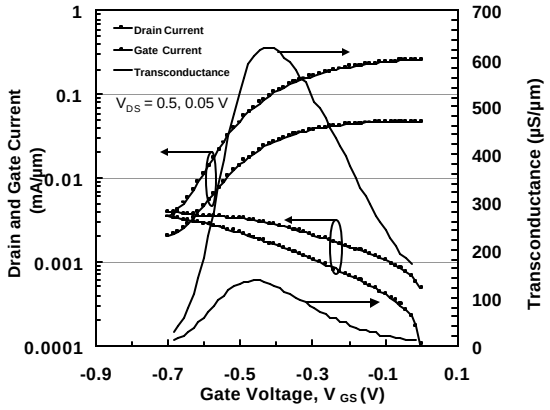

Figure 6. 0.2 µm L_G InSb QW transistor transfer characteristics at 295 K, Type A material, L_{DS} = 2 µm, W_G = 80 µm, V_{DS} = 0.5 V, 50 mV.

Figure 6 shows the transfer characteristics of the device at V_{DS} = 0.5 V and 50 mV. The peak g_m for this device is 625 µS/µm at V_{DS} = 0.5 V. The device shows an on-current of 263 µA/µm, off-current of 3.4 µA/µm, and a sub-threshold slope of 142 mV/decade at V_{DS} = 0.5 V. The off-state current is limited by gate (non-optimized) to drain leakage as indicated in Figure 6. Using higher Al percentage barriers allows the barrier to be thinned, improving g_m and subthreshold slope. Figure 7 shows the preliminary DC results of a 0.2 µm InSb quantum well transistor fabricated with Type B material with a 20 nm 30% Al barrier layer and mobility of 32,000 cm $^2V^{-1}s^{-1}$ at $n_s = 1.3\times10^{12}$ cm^{-2}. The device shows an on-state current of 275 µA/µm, off-current of 4.1 µA/µm, and a sub threshold slope of 110 mV/decade at V_{DS} = 0.5 V. The peak g_m for this device is 920 µS/µm at V_{DS} = 0.5V.

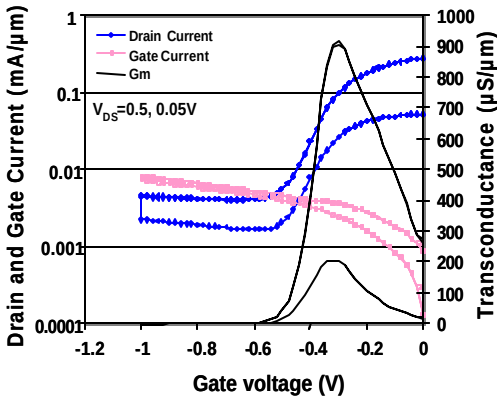

Figure 7. 0.2 µm L_G InSb QW transistor transfer characteristics at 295 K, Type B material, L_{DS} = 2 µm, W_G = 80 µm, V_{DS} = 0.5 V, 50mV.

5. High Frequency Characterization

RF characteristics of the Type A InSb transistors were obtained at room temperature through on-wafer S-parameter measurements at frequencies up to 50 GHz by using an HP 8510C vector network analyzer. Figure 9 shows the frequency dependence of the short circuit current gain $|h_{21}|$, MAG/MSG and Mason's unilateral power gain U_g for the 0.2 µm gate length InSb transistor at V_{DS} = 0.5 V and V_{GS} = -0.4 V. The parasitic capacitances associated with the probe pads were subtracted from the measured S-parameters through a two-step de-embedding process. We obtain an f_T of 150 GHz by extrapolating $|h_{21}|^2$ with a slope of –20 dB/decade using a least squares fit. The maximum oscillation frequency f_{max} is around 190 GHz from both MSG/MAG and U_g, yielding an f_{max}/f_T ratio of 1.3. Figure 10 compares the high frequency (f_T)

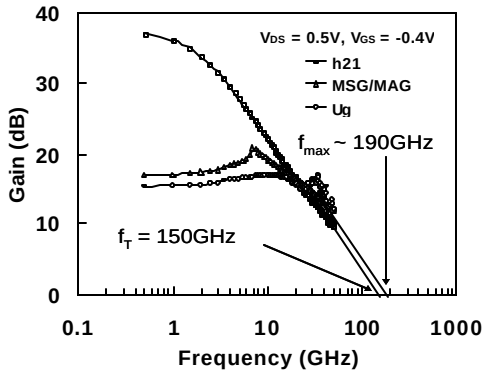

Figure 9. Intrinsic current gain $|h_{21}|$, MSG/MAG and Mason's gain U_g (after de-embedding) versus frequency for 0.2 µm InSb quantum well device with V_{DS} = 0.5 V and V_{GS} = -0.4 V.

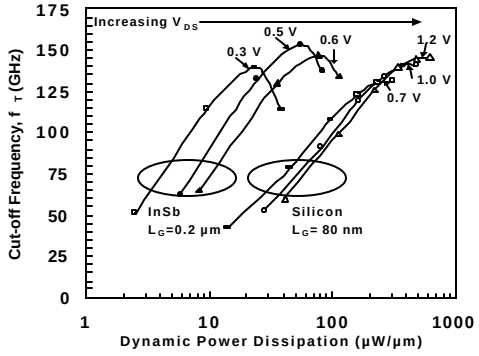

Figure 10. Extrapolated f_T vs dynamic power dissipation (normalized to transistor width) for InSb QW transistors (solid) for L_G = 0.2 µm and state-of-the-art Si nMOS transistors (open) for L_G = 80nm.

and dynamic power dissipation performance of state-of-the-art Si nMOSFETs (80 nm L_G) with the InSb based quantum well FET's (0.2 µm L_G). The InSb transistors provide equivalent high-speed performance (f_T) at 5 to 10 times lower power dissipation per unit width compared to today's advanced Si RF MOSFETs [2], as shown in Figure 10. This makes the InSb-based device technology a viable option for future generation ultra-high speed, very low power digital and RF applications. Future challenge is to scale the gate length of InSb transistors to compete with scaled CMOS transistors [3] for ULSI applications while maintaining the power advantage. Figure 11 shows the gate delay (CV/I) of InSb and state-of-the-art and research Si transistors as a function of gate length, showing the performance advantage at equivalent gate length.

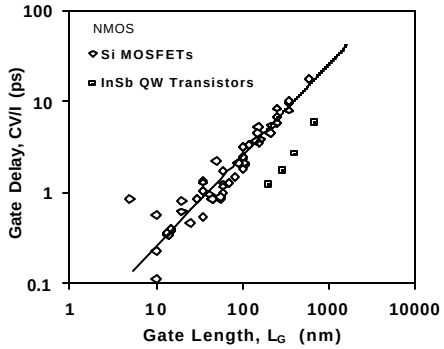

Figure 11. Transistor gate delay (CV/I) vs gate length for InSb QW transistors at V_{DS} = 0.5 V bench-marked against state-of-the-art Si nMOS transistors.

6. Conclusion

In summary, we have demonstrated for the first time InSb quantum well transistors down to 0.2 µm gate length with comparable high frequency performance to today's Si MOSFET's but with 5-10 times lower dynamic power dissipation. This is enabled by lowering the supply voltage to 0.5 V due to 50X higher room-temperature mobility in InSb compared to silicon.

References

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