Emerging Silicon and Non-Silicon Nanoelectronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications (Invited Paper)

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ABSTRACT

Several key emerging nanoelectronic devices, such as Si nanowire field-effect transistors (FETs), carbon nanotube FETs, and III-V compound semiconductor quantum-well FETs, are assessed for their potential in future high-performance, low-power computation applications. Furthermore, these devices are benchmarked against state-of-the-art Si CMOS technologies. The two fundamental transistor benchmarking metrics utilized in this study are (i) CV/I versus L_G and ii) CV/I versus I_{ON}/I_{OFF}. While intrinsic device speed is emphasized in the first metric, the tradeoff between device speed and off-state leakage is assessed in the latter. For high-performance and low-power logic applications, low CV/I and high I_{ON}/I_{OFF} values are both required. Based on the results obtained, the opportunities and challenges for these emerging novel devices in future logic applications are highlighted and discussed.

I. INTRODUCTION

According to Moore's Law, the number of transistors per integrated circuit doubles every 24 months, and it has been the guiding principle for the semiconductor industry for over 30 years. The sustaining of Moore's Law, however, requires continued transistor scaling and performance improvements. The physical gate length L_G of the Si transistors used in the 90 nm logic generation node is ~ 50 nm. It is projected that transistor L_G will reach ~ 10 nm in 2011. By way of innovation in silicon technology, such as strained-Si channels [1, 2], high-κ/metal-gate stacks [3–5], and the non-planar Tri-gate CMOS transistor architecture [6], CMOS transistor scaling and performance will continue at least until the middle of the next decade. Recently, a lot of interest generated has been generated and good progress has been made in the study of novel silicon and non-silicon nanoelectronic devices, including Si-nanowire field-effect transistors (FETs) [7–11], carbon-nanotube FETs (CNTFETs) [12–18], and III-V compound semiconductor quantum-well FETs (QWFETs) [19, 20], in the capacity of future computation applications. These devices hold promise as candidates for integration with the ubiquitous silicon platform in order to enhance circuit functionality while simultaneously enabling the extension of Moore's Law well into the next decade and beyond. In this work, two fundamental device metrics, namely (i) CV/I versus L_G and (ii) CV/I versus I_{ON}/I_{OFF}, are used to benchmark these emerging nano-electronic devices vis-à-vis state-of-the-art Si CMOS transistors with regard to high-performance, low-power logic CMOS-like applications. These benchmarking metrics and corresponding methodologies have previously been described in great detail [21, 22]. While the first metric highlights the intrinsic speed of devices, the latter permits an assessment of the tradeoff between device intrinsic speed and off-state leakage. Data from our own research devices and also from literature were used in this study. The merits and potential shortcomings of these emerging devices will be discussed. Figure 1 shows the images of some of the novel research transistors discussed in this work.

II. EMERGING P-CHANNEL NANOELECTRONIC DEVICES

The room temperature CV/I versus L_G comparison of conventional Si transistors, Si nanowire transistors, and CNT transistors with p-channels is shown in Figure 2. The data indicate that CNTs exhibit significant CV/I improvement when compared to conventional Si devices. This improvement is due primarily to the mobility enhancement in CNTs. By contrast, the CV/I characteristics of Si nanowire devices and conventional Si devices are similar. A recent report suggests that, fundamentally, there is no reason to expect Si nanowire transistors to have higher channel mobility than standard planar Si devices at room temperature [23]. For example, TCAD simulations have shown that phonon scattering increases, and

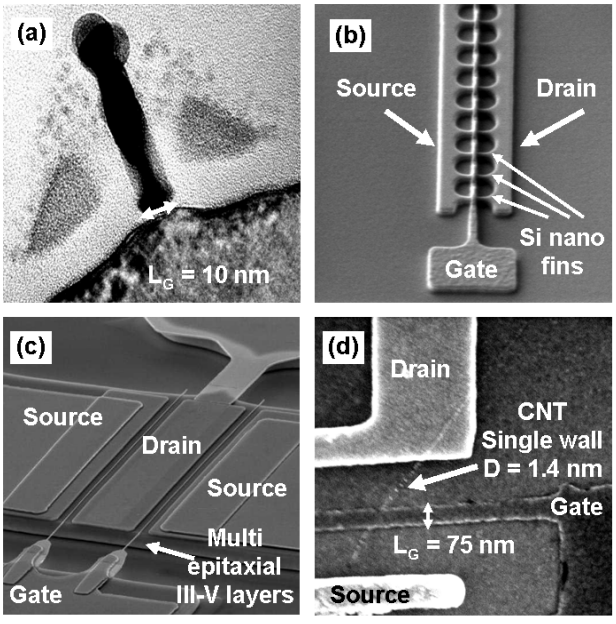

FIGURE 1. TEM cross-section and SEM images of research transistors. (a) Planar Si MOSFET with physical gate length L_G = 10 nm, (b) non-planar Si Tri-gate transistor with multiple Si nano fins, (c) a III-V quantum well FET on a multi-layered epitaxial substrate, and (d) a top-gated CNTFET.

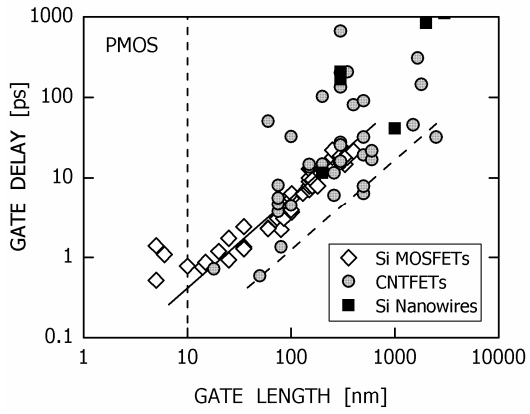

FIGURE 2. Gate delay (intrinsic device speed) *CV/I* versus transistor physical gate length L_G of PMOS devices. The diameters of the CNTs are within the 1.0-2.5 nm range while those of the Si nanowires are within the 4-35 nm range.

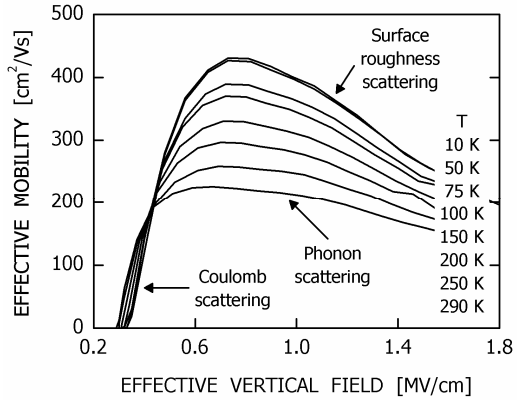

FIGURE 3. Effective electron mobility μ_{eff} as a function of effective vertical field E_{eff} of a Si nano-fin structure in the temperature range T = 10-290 K. Note that the T = 10 and 50 K curves overlap each other. The primary scattering mechanisms: phonon scattering, surface-roughness scattering, and Coulomb scattering, are identified on the plot. The impact of phonon scattering becomes significant above 50 K. At effective fields of interest, the effective mobilities at higher temperatures are lower than those at lower temperatures.

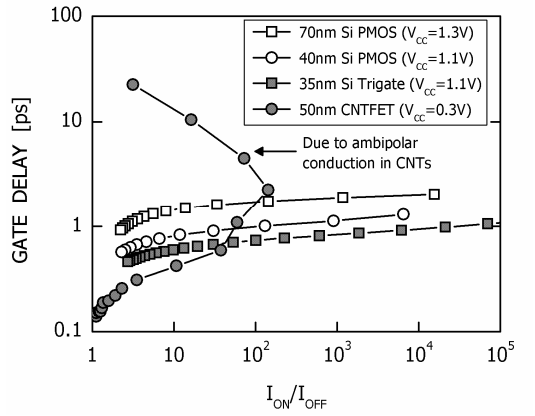

FIGURE 4. Gate delay (intrinsic device speed) *CV/I* versus on-to-off state current ratio I_{ON}/I_{OFF} of Si PMOS transistors with physical gate length L_G = 70 nm at supply voltage V_{CC} = 1.3 V and L_G = 40 nm at V_{CC} = 1.1 V, a Si Trigate PMOS transistor with L_G = 35 nm at V_{CC} = 1.1 V, and a CNT PMOS transistor with L_G = 50 nm at V_{CC} = 0.3 V [17]. The I_{ON}/I_{OFF} ratio in CNTFETs is limited by the ambipolar conduction.

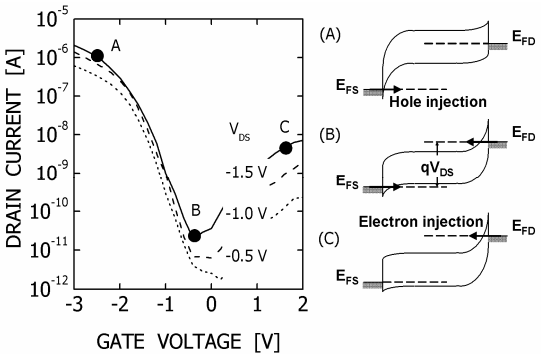

FIGURE 5. I_D-V_G characteristics of a carbon nanotube PMOS transistor with Pd metal source-drain at different drain biases V_{DS}, illustrating ambipolar conduction. Pd has a p-type work function with respect to nanotubes. The energy band diagrams exhibit (A) dominant hole injection in the on-state, (B) equal hole and electron injection at the minimum current point, and (C) dominant electron injection in the ambipolar branch.

hence the phonon-limited mobility decreases, at room temperature for devices containing Si nanowires with diameters less than 15 nm [23]. Additionally, experimental studies reveal that while phonon scattering in Si nanostructures is suppressed at low temperatures, phonon scattering limited transport is indeed prevalent at room temperature, limiting effective channel mobility, as shown in Figure 3. Hence, at room temperature, Si nanowires with dimensions of interest for scaling do not exhibit transistor performance enhancement when compared to conventional planar Si architectures, as shown in Figure 2.

The p-channel *CV/I* versus I_{ON}/I_{OFF} characteristics of the CNT-FET are shown in Figure 4. Included in this figure are data from conventional planar Si and non-planar Tri-gate Si transistors for comparison. Despite the observation that CNTFETs exhibit high intrinsic speed (*CV/I*) performance, as shown in Figure 2, they in fact suffer from a low I_{ON}/I_{OFF} ratio. This low ratio is attributed to a high I_{OFF} for the CNTFET, as shown in Figure 5, which in turn is due to the existence of ambipolar leakage [15, 21, 22]. The ambipolar leakage is a consequence of metal-CNT Schottky contacts, which are used instead of standard implanted or diffused p-n junctions. It is anticipated that the use of standard p-n junctions will eliminate ambipolar leakage and improve the I_{ON}/I_{OFF} ratios of CNTFETs. It is noted, however, that for high-performance and low-power logic applications, both low *CV/I* and high I_{ON}/I_{OFF} values are required.

III. EMERGING N-CHANNEL NANOELECTRONIC DEVICES

Figure 6 shows the room temperature *CV/I* versus L_G comparison of conventional Si transistors, CNT transistors, and III-V (InSb) compound semiconductor QW transistors [19, 20] with n-channels. In comparison with conventional Si devices, InSb transistors exhibit significantly larger n-channel intrinsic speed (*CV/I*), a benefit of higher channel mobility and lower utilized supply voltage V_{CC} (0.5 V). The increased channel mobility also translates to a high-frequency gain in InSb transistors, as shown in Figure 7 [20]. In this case, the dc *CV/I* data is directly correlated to the ac cutoff-frequency f_T data.

The n-channel CNT devices in Figure 6 all show degraded *CV/I* performance compared to conventional Si n-channel devices. This

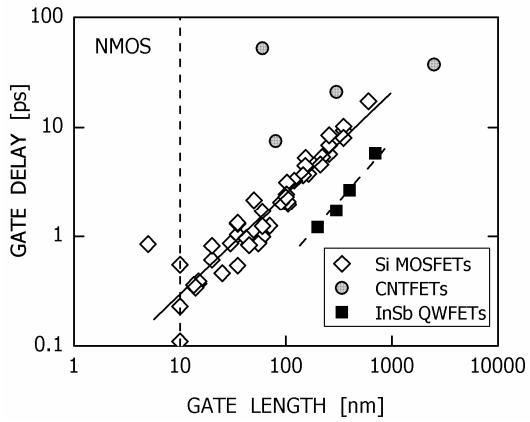

FIGURE 6. Gate delay (intrinsic device speed) *CV/I* versus transistor physical gate length L_G of NMOS devices. The diameters of the CNTs are within the 1.0-2.5 nm range.

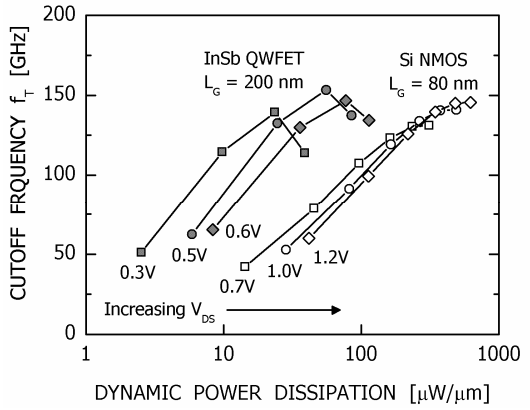

FIGURE 7. Cutoff frequency f_T versus dynamic power dissipation of an n-channel InSb QWFET with gate length L_G = 200 nm and a Si NMOS with L_G = 80 nm at different values of drain bias V_{DS}. f_T is obtained from high-frequency measurement of transistor *s*-parameters [20].

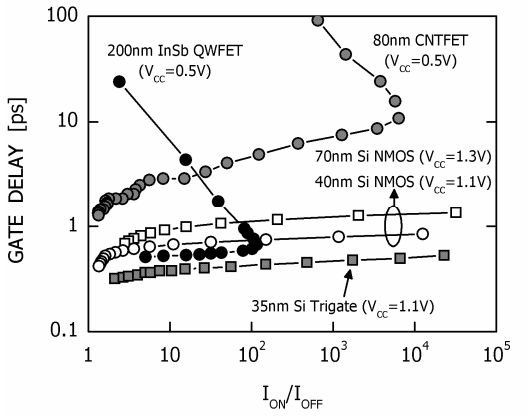

FIGURE 8. Gate delay (intrinsic device speed) *CV/I* versus on-to-off state current ratio I_{ON}/I_{OFF} of Si NMOS transistors with physical gate length L_G = 70 nm at supply voltage V_{CC} = 1.3 V and L_G = 40 nm at V_{CC} = 1.1 V, a Si Trigate NMOS transistor with L_G = 35 nm at V_{CC} = 1.1 V, an InSb n-type quantum-well FET (QWFET) with L_G = 200 nm at V_{CC} = 0.5 V [20], and a CNT NMOS transistor with L_G = 80 nm at V_{CC} = 0.5 V [18]. The use of chemically-doped junctions [18] delays the ambipolar conduction in the CNTFET, despite poor gate delay performance. Nevertheless, this represents a major breakthrough in CNTFET research [18]. The I_{ON}/I_{OFF} ratio of the InSb QWFET is limited by Schottky gate leakage [20].

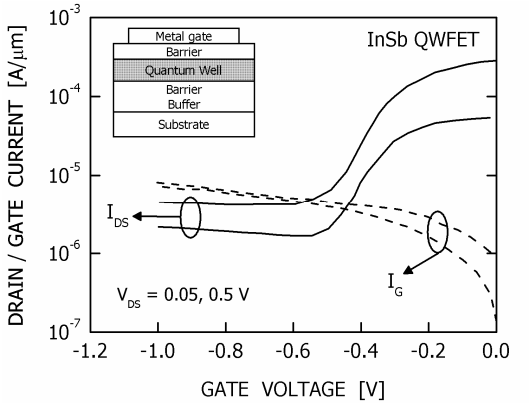

FIGURE 9. Drain current I_{DS} and gate leakage current I_G versus gate voltage V_{GS} of an InSb n-type quantum-well FET (QWFET) with physical gate length L_G = 200 nm. Inset: Schematic of device layers in III-V material-based QWFETs with Schottky metal gates. I_G is the Schottky gate leakage due to the absence of gate dielectric [20].

phenomenon can possibly be explained by considering that a suitable n-type workfunction metal that forms a stable interface with CNTs has yet to be demonstrated. Upon resolution of this issue, a high performance n-channel CNTFET is anticipated based on the symmetry of the conduction and valence bands for CNTs [24].

In Figure 8, n-channel *CV/I* versus I_{ON}/I_{OFF} characteristics are shown for CNTFETs with chemically-doped junctions [18] and for InSb QWFETs. Also shown, for the sake of direct comparison, are conventional planar Si and non-planar Tri-gate Si transistors. The use of chemically-doped junctions in CNTFETs [18], as opposed to metal-CNT Schottky junctions, suppresses the ambipolar leakage conduction and reduces I_{OFF}, thus improving the I_{ON}/I_{OFF} ratio. However, the resulting *CV/I* performance is still degraded, possibly due to increased external parasitic resistance of the doped junctions. Nevertheless, this chemically-doped junction approach is indeed a major advancement for CNTFET research [18].

Interestingly, the n-channel InSb QWFET also exhibits a low I_{ON}/I_{OFF} ratio, as shown in Figure 8. This phenomenon is a consequence of high gate leakage, as exhibited in Figure 9, due to the low barrier height at the Schottky metal-semiconductor junction. The low barrier height arises from (a) Fermi-level pinning at the metal-semiconductor interface and (b) the use of a narrow-bandgap semiconductor. It is predicted that the use of a gate dielectric between the metal gate and the III-V device layers will eliminate such Schottky gate leakages and improve the I_{ON}/I_{OFF} ratio [20].

IV. CONCLUSIONS

In this paper, we have identified the merits and potential shortcomings of various emerging nanoelectronic devices with respect to future logic applications. Specifically, we have shown that (a) Si nanowires offer no transistor *CV/I* performance advantage over conventional Si transistors at room temperature, likely due to the significant role played by phonon scattering at room temperature, and that (b) both p-channel CNTFETs and n-channel QWFETs exhibit impressive *CV/I* gain when compared against conventional Si transistors, but they suffer from degraded I_{ON}/I_{OFF} ratios, a result of ambipolar conduction and Schottky gate leakage, respectively. Based

on this study, we anticipate that upon solving the off-state leakage problems, high-mobility devices such as CNTFETs and III-V QWFETs have the potential to enable high-performance logic applications with very low supply voltage V_{CC} (e.g. below 0.5 V).

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