# Gate Dielectric Scaling for High-Performance CMOS: from SiO2 to High-K


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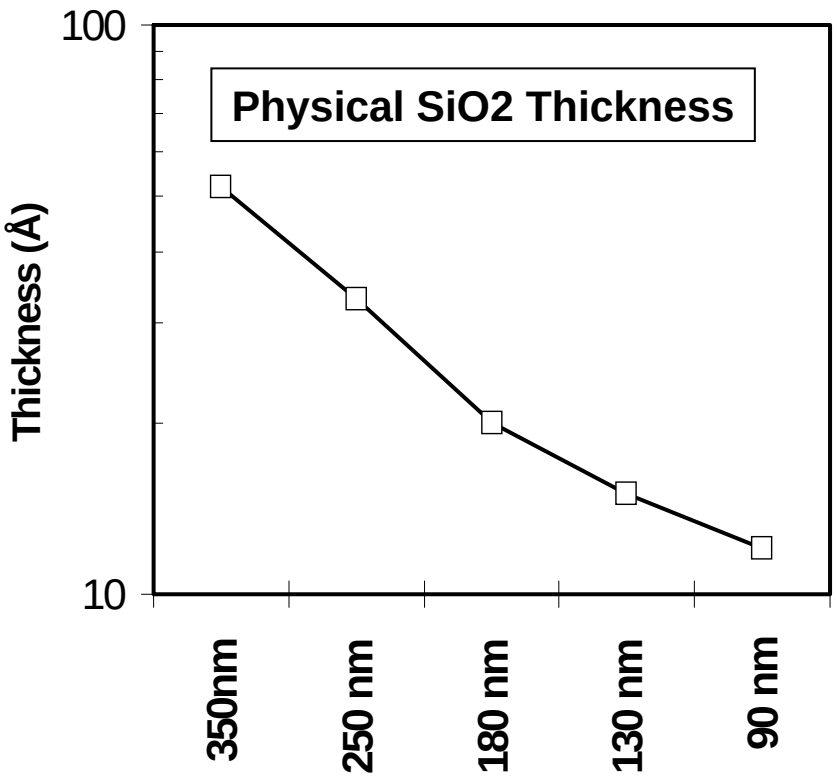
# Content

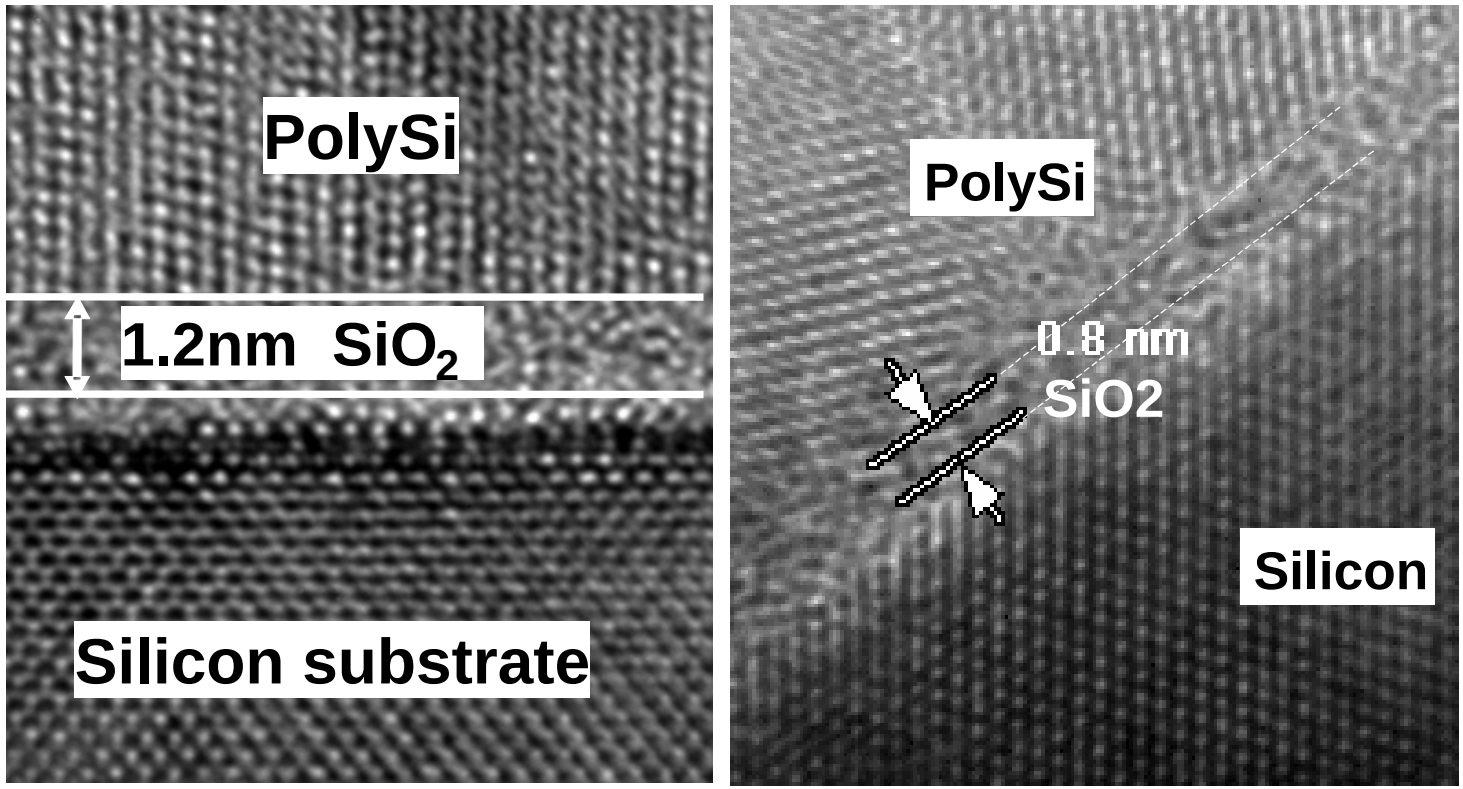
- **Introduction**
- **SiO2 Scaling**
- **Review on High-K Problems**
- **Significant Breakthroughs in High-K/Metal-Gate**
- **High-K/Metal-gate NMOS & PMOS Transistors with Record-Setting Drive Performance**
- **Summary**

# Introduction



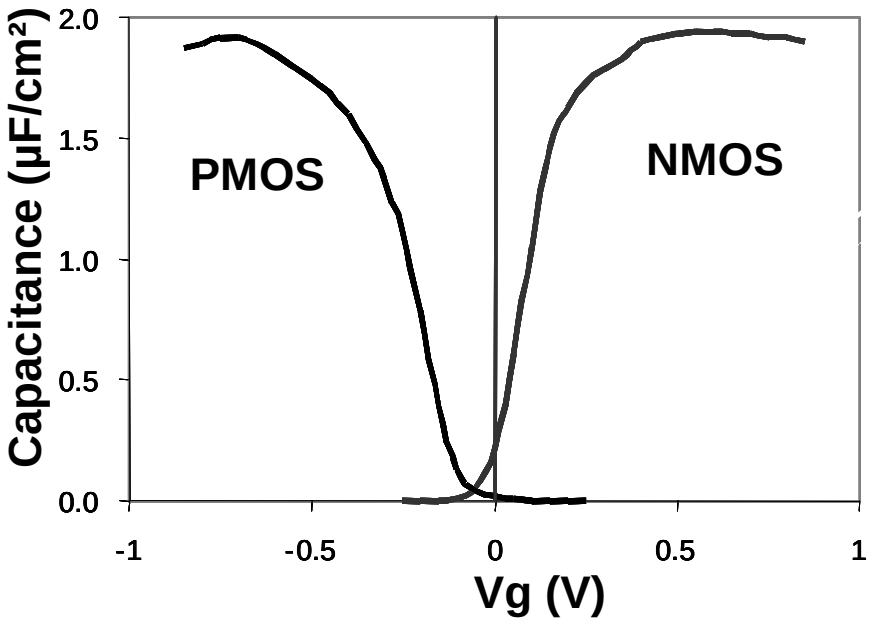

- **1.2nm physical SiO2 in production in our 90nm logic technology node**
- **0.8nm physical SiO2 in our research transistors with 15nm physical Lg**
- **Gate leakage is increasing with reducing physical SiO2 thickness**
- **SiO2 running out of atoms for further scaling**
- **Will eventually need high-K**

# SiO2 Scaling

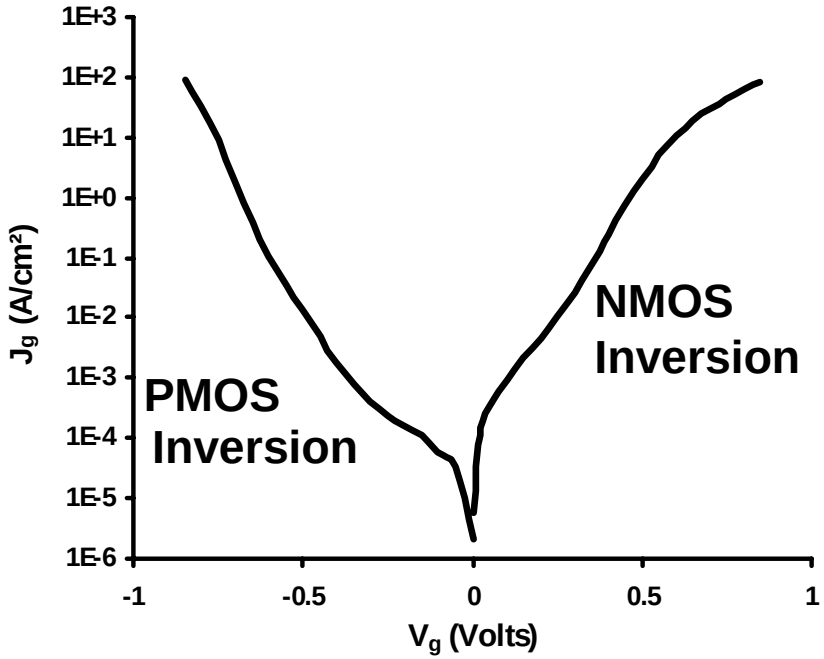



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

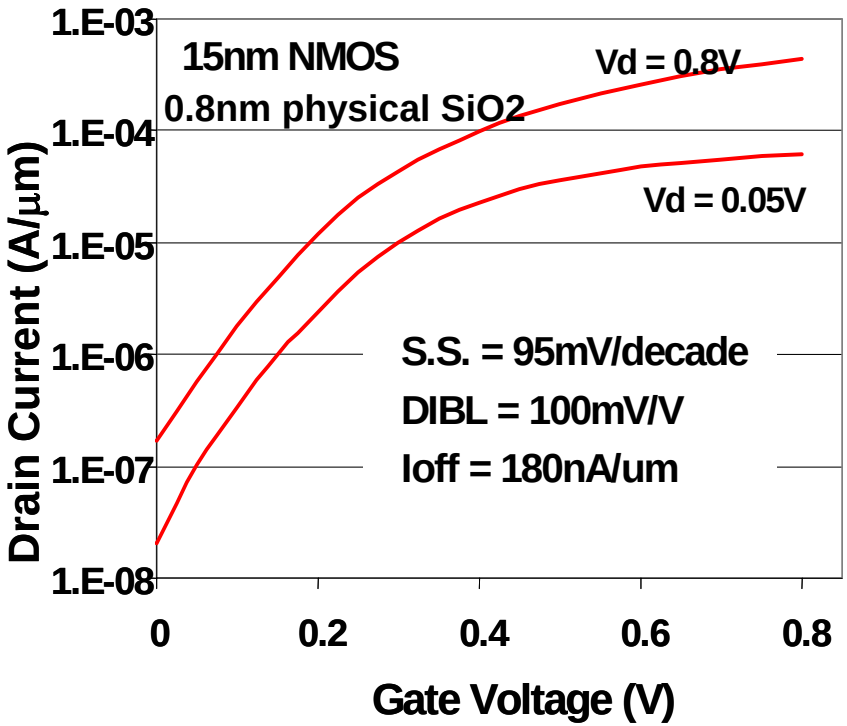
# Electrical Characteristics of 0.8nm Physical SiO2

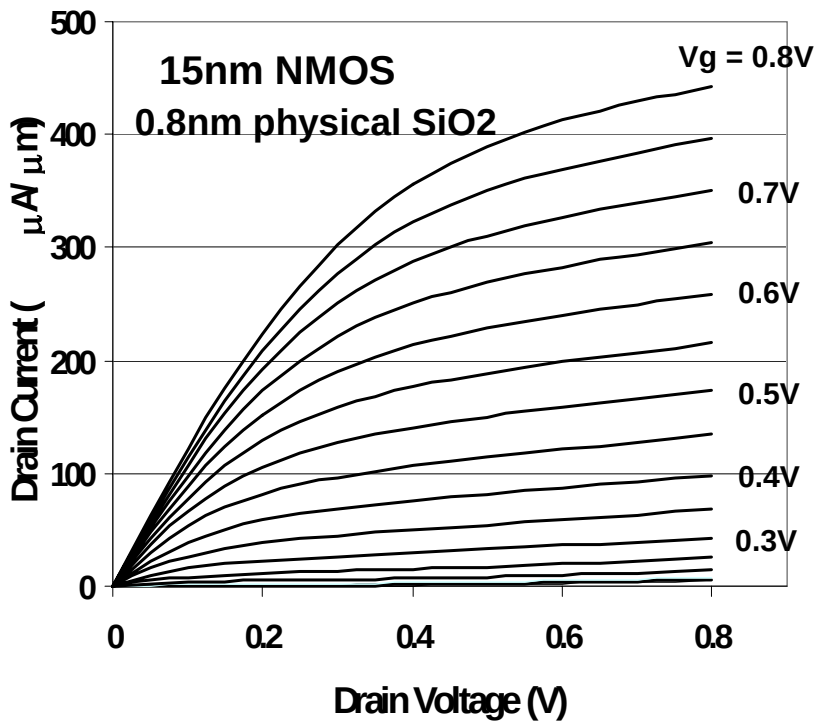



**Inversion Capacitance**



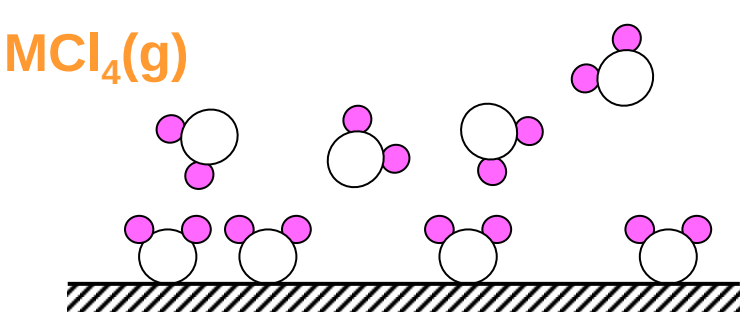
# Research Transistor with 15nm Physical Lg and 0.8nm Physical SiO2



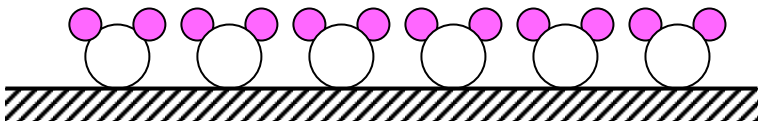




- **Well-controlled short-channel characteristics**

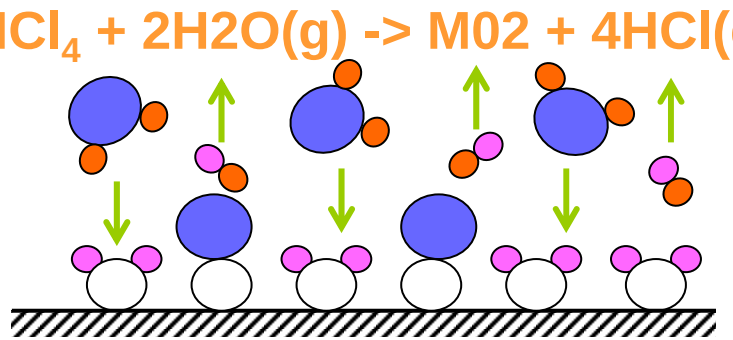
# Formation of High-K: Atomic Layer Deposition



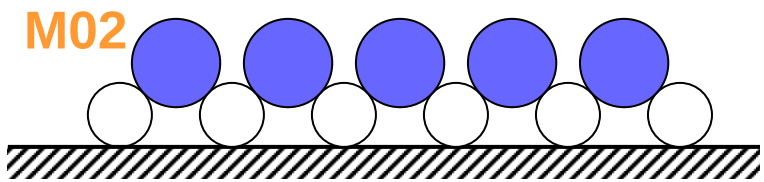

Step 1



Step 2




Step 3




Step 4

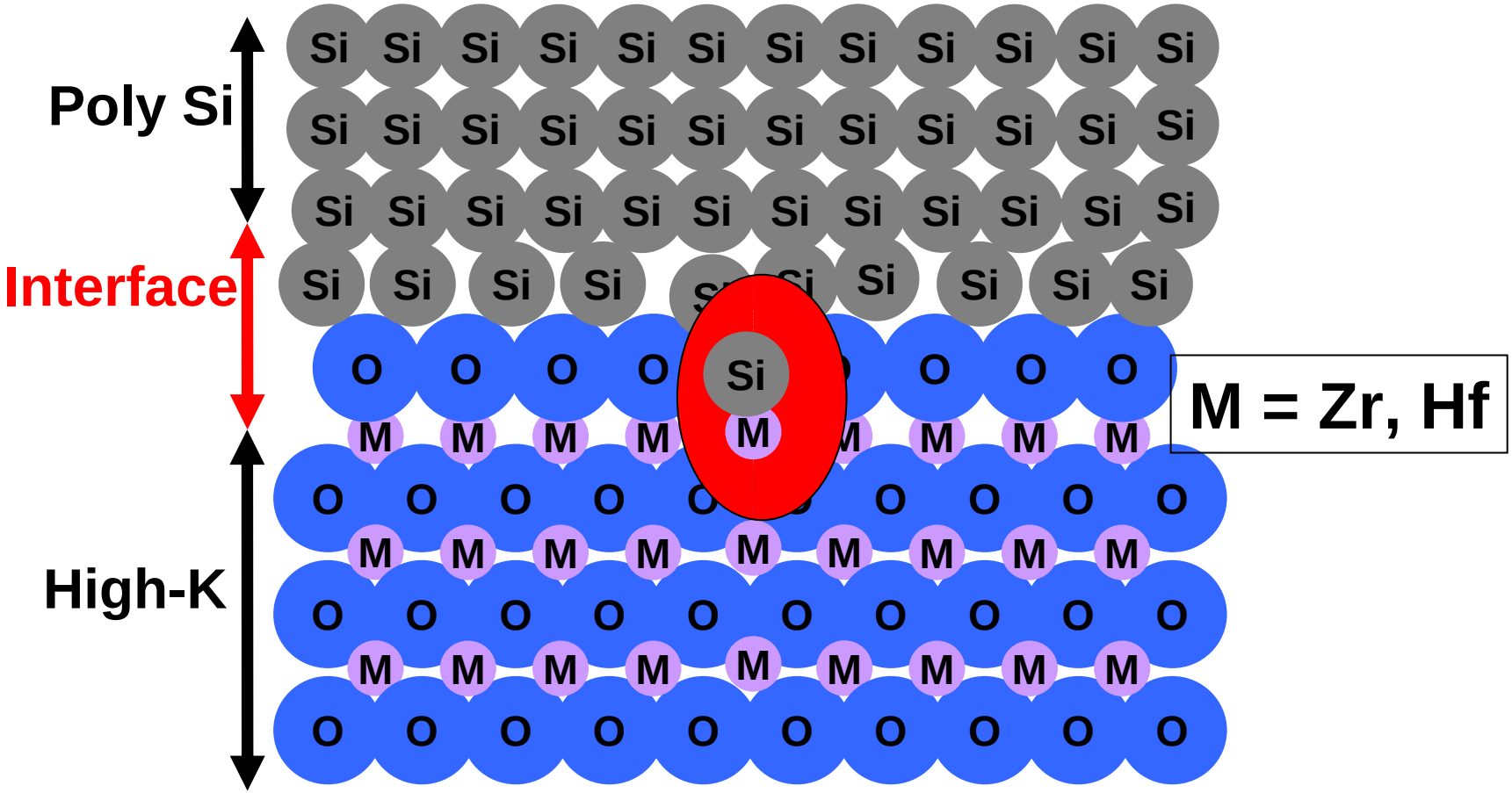
**M = Zr, Hf**

- **Sequential introduction of precursor molecules $MCl_4(g)$, $H2O(g)$**

# Review on High-K Problems (High-K/PolySi-Gate)

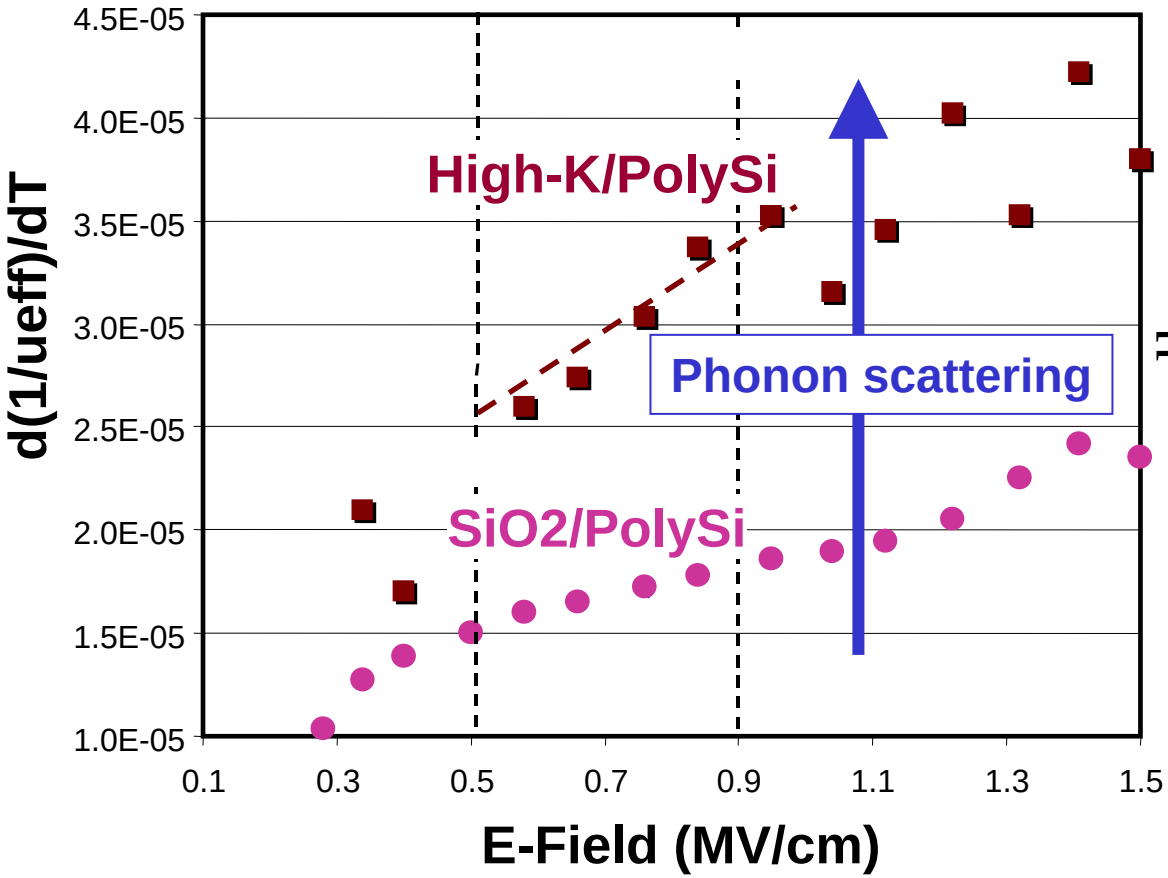
- **High-K and polySi gate are incompatible due to Fermi level pinning at the high-K and polySi interface which causes high threshold voltages in transistors**
- **High-K/polySi transistors exhibit severely degraded channel mobility due to the coupling of SO phonon modes in high-K to the inversion channel charge carriers**

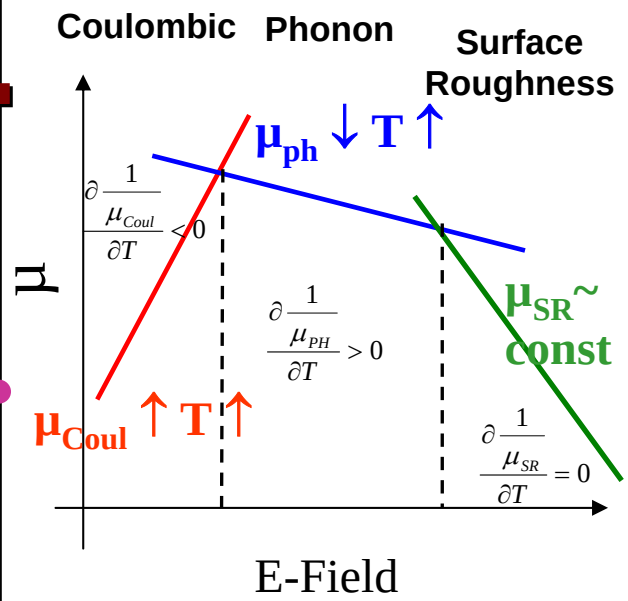
# High-K and PolySi are Incompatible




- Defect formation at the polySi-high-K interface

# Experimental Evidence of Phonon Scattering in High-K




$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{Coul}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{SR}}$$

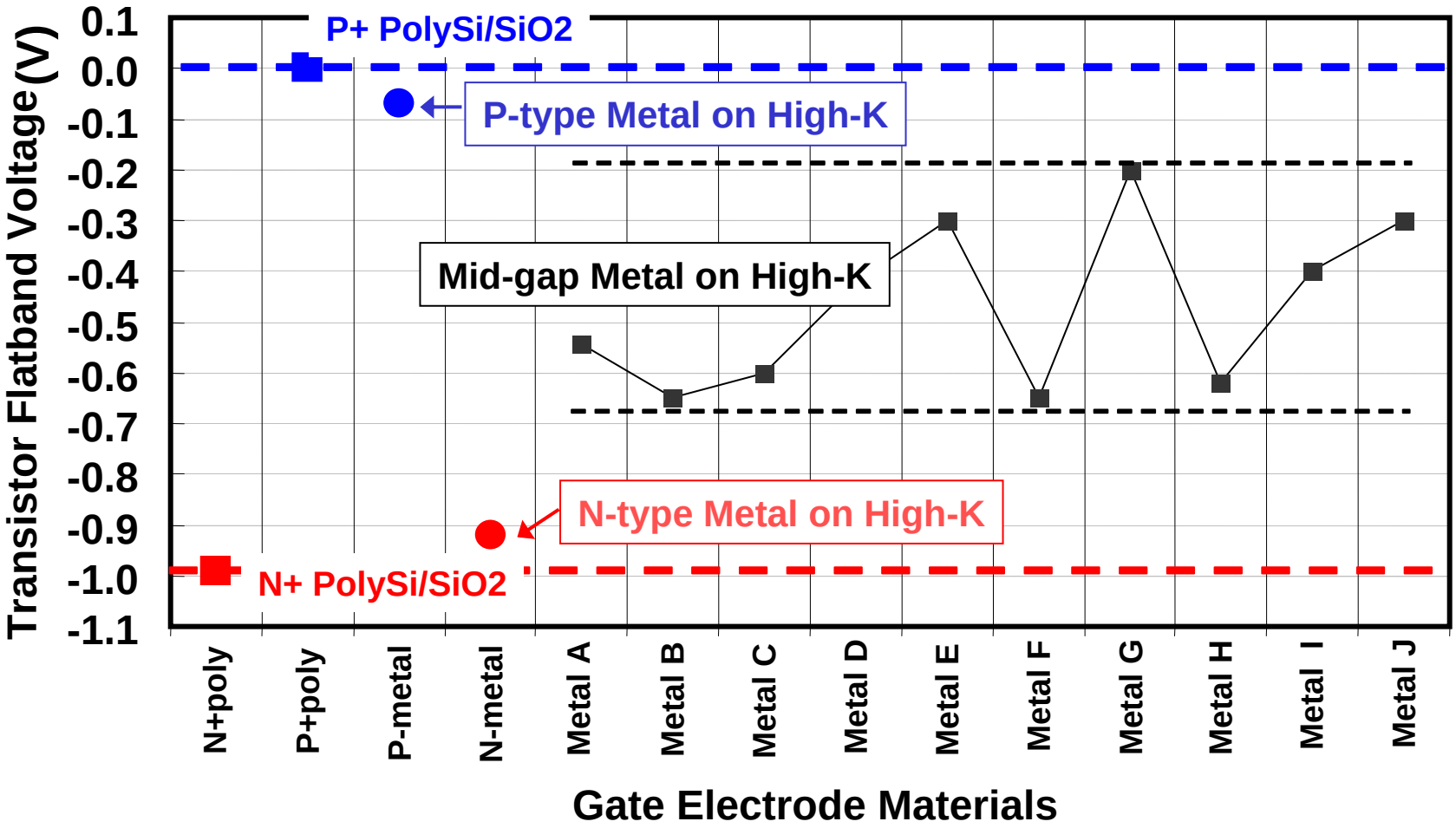
# Review on High-K Problems (High-K/Metal-Gate)

- **Metal gate electrodes may be able to screen the high-K SO phonons from coupling to the inversion channel charge carriers and reduce the mobility degradation problem**
- **However the use of high-K/metal-gate requires metal gate electrodes with the "correct" work functions on high-K for both PMOS and NMOS transistors for high performance**

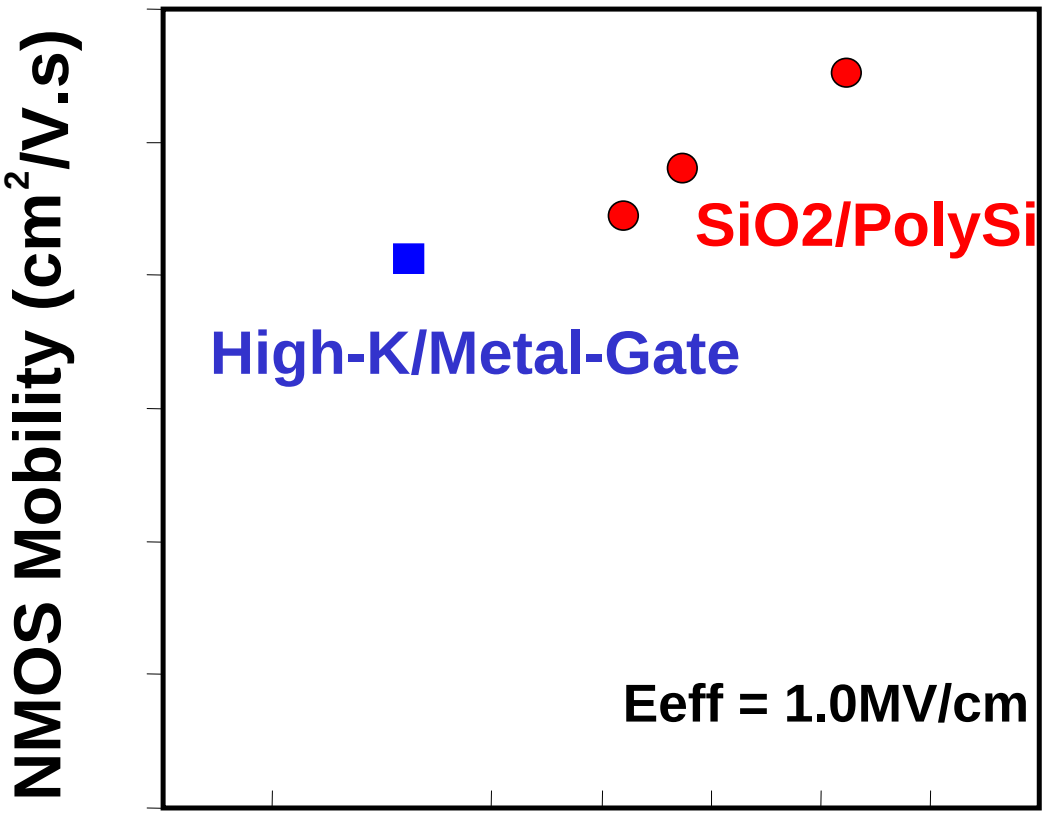
# Significant Breakthroughs in High-K/Metal-Gate made by Intel

- **N-type metal and P-type metal with the correct work functions on high-K have been engineered and demonstrated for high-performance CMOS**
- **High-K/metal-gate stack achieves NMOS and PMOS channel mobility close to SiO2's**
- **High-K/metal-gate stack shows significantly lower gate leakage than SiO2**

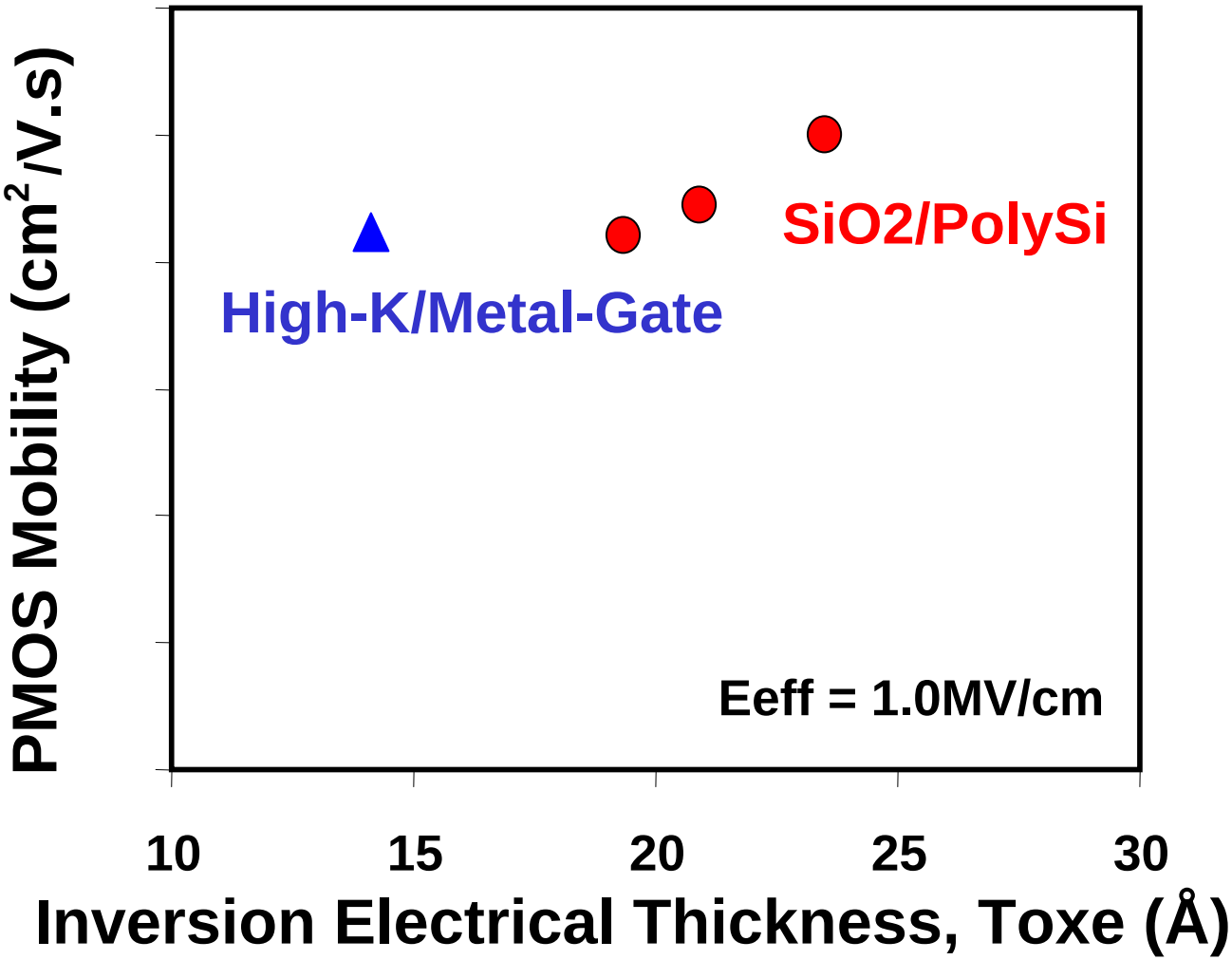
# We have Engineered N-type and P-type Metal Electrodes on High-K with the "Correct" Work Functions for NMOS and PMOS on Bulk Si



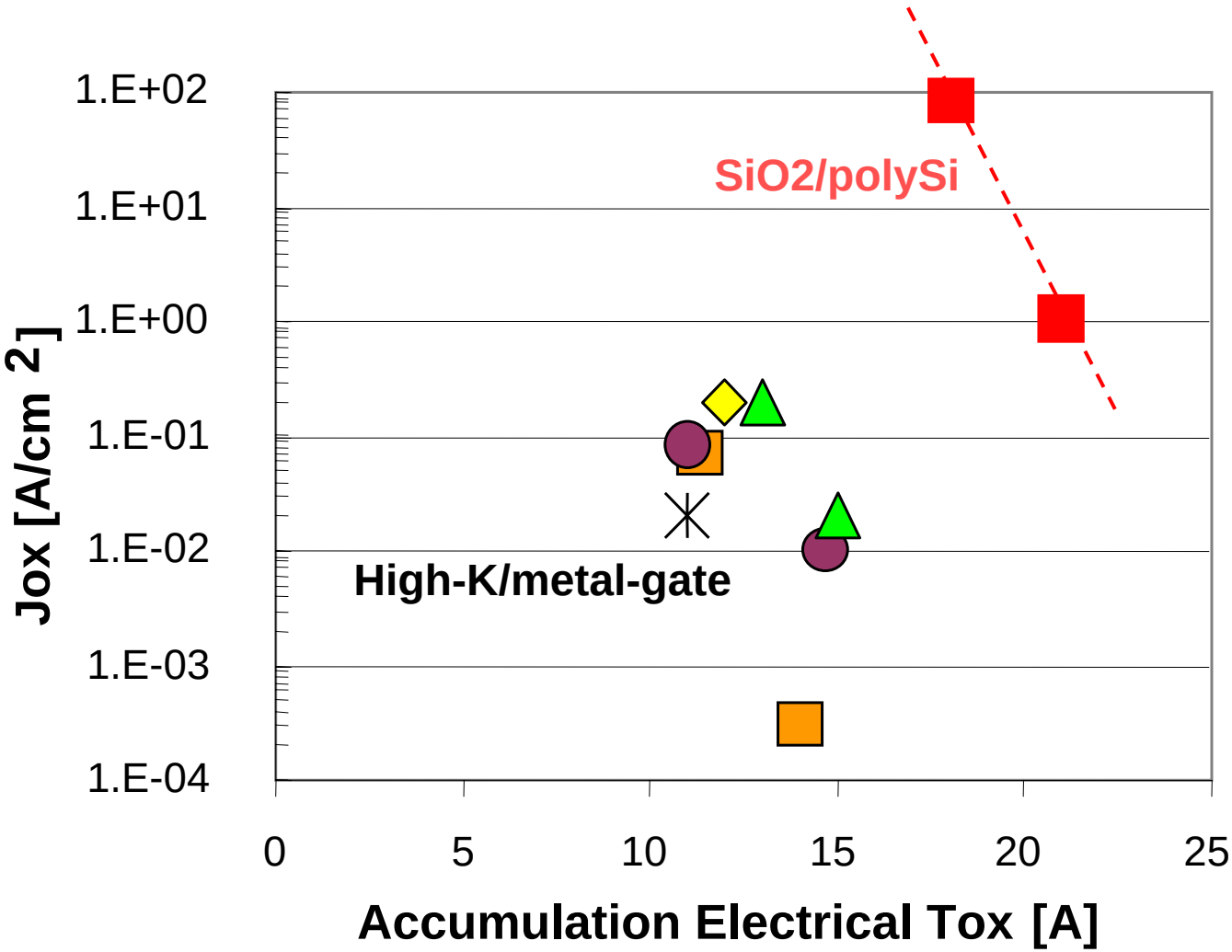
# High-K/Metal-Gate Stack Achieves NMOS Channel Mobility Close to SiO2



# High-K/Metal-Gate Stack Achieves PMOS Channel Mobility Close to SiO2



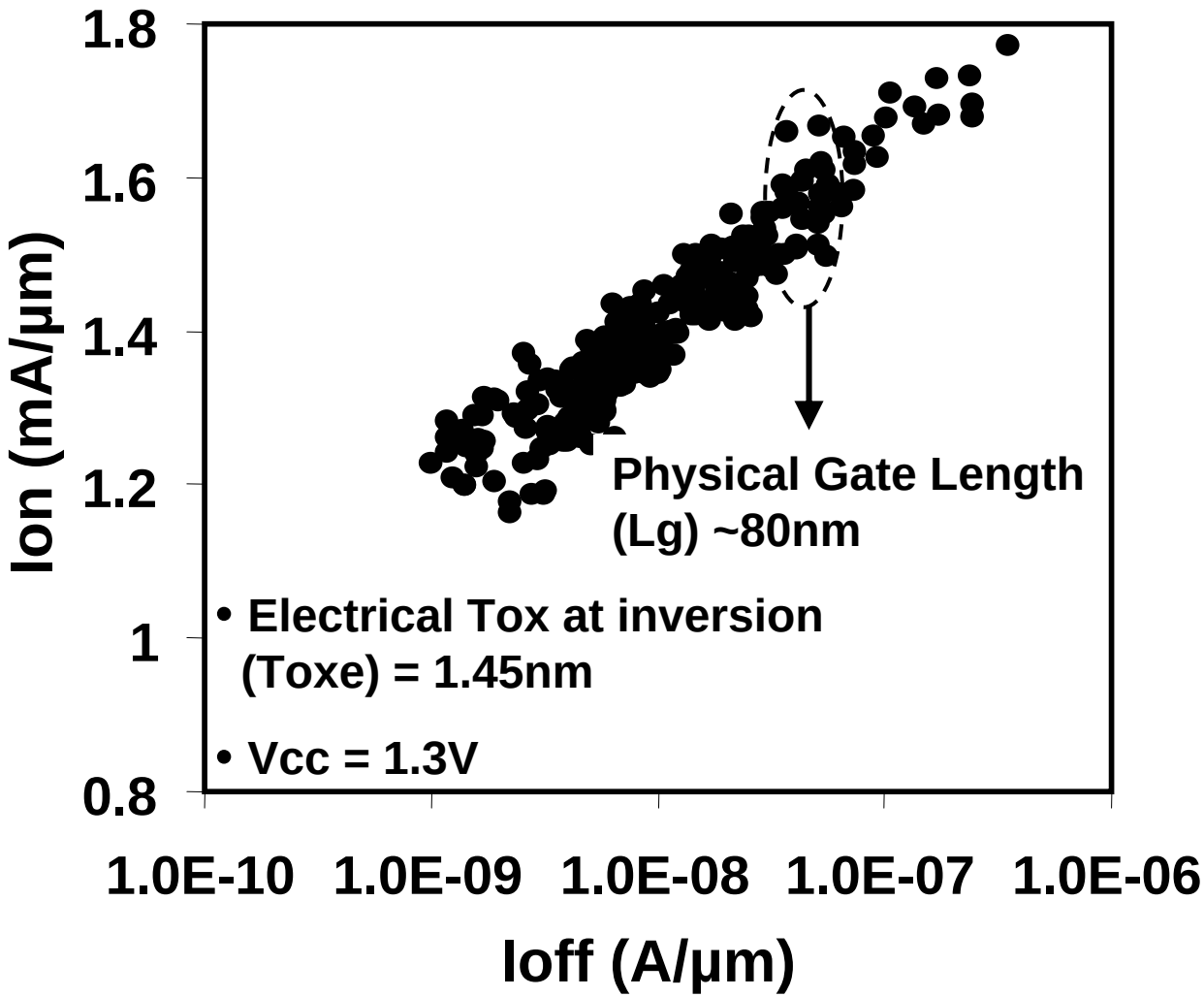
# High-K Reduces Gate Leakage



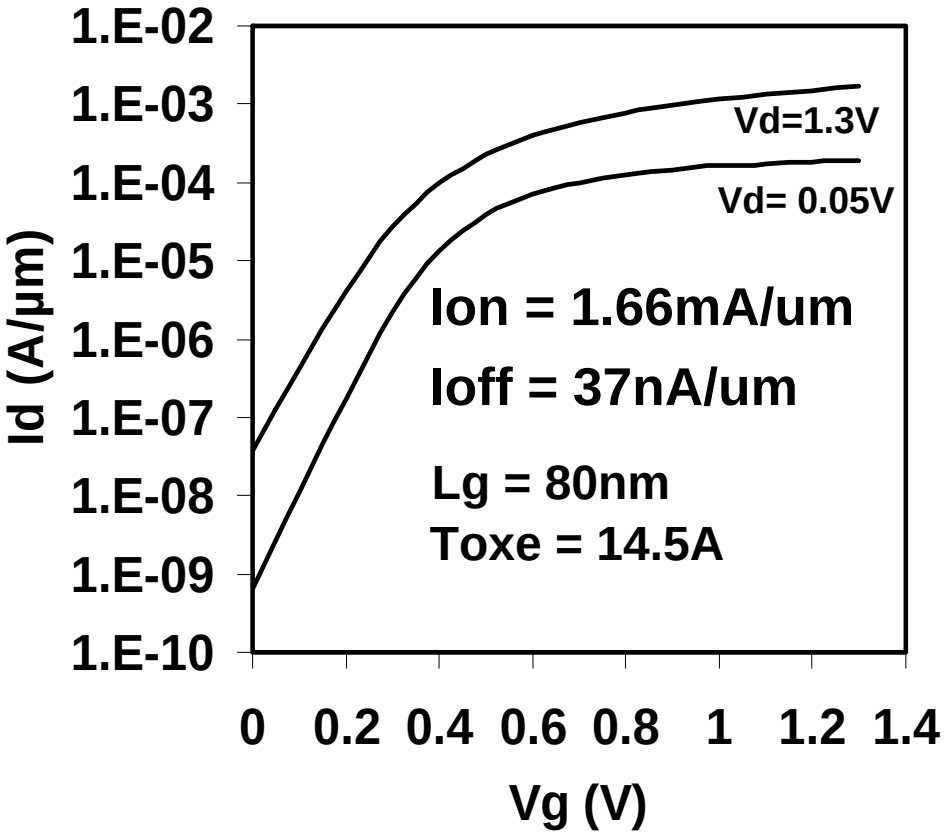
# High-K/Metal-gate NMOS and PMOS Transistors with Record-Setting Drive Current (Idsat) Performance

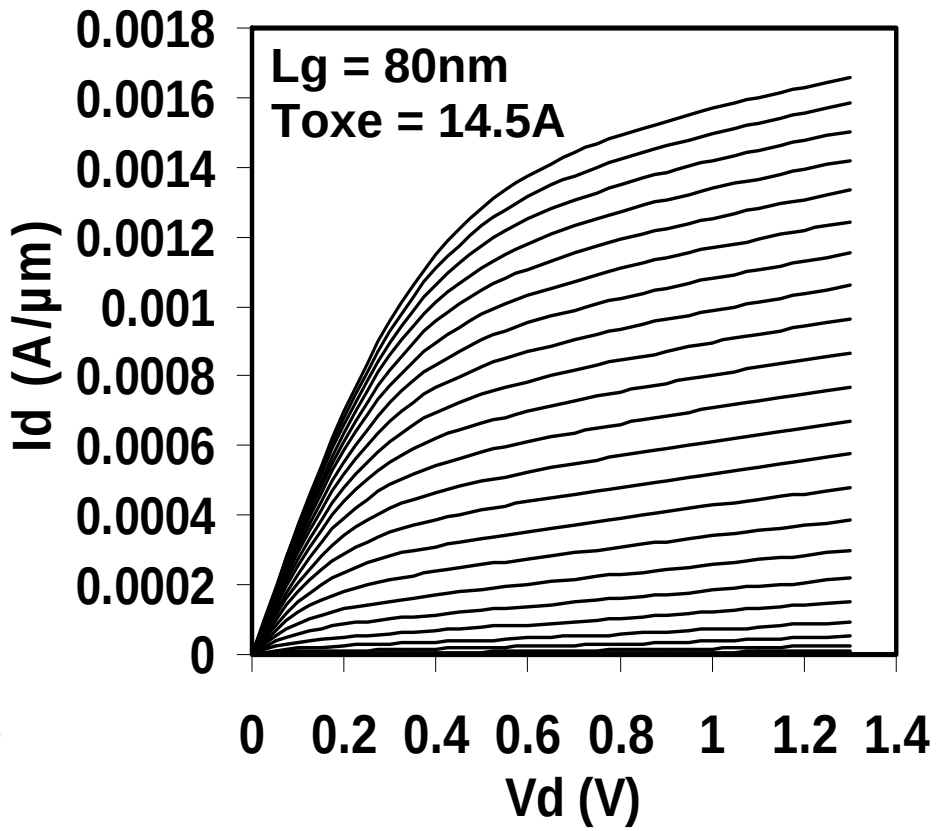
- **NMOS and PMOS high-K/metal-gate transistors were made on bulk Si**
  - **Physical gate length (Lg) = 80nm**
  - **Electrical Oxide Thickness @ inversion (Toxe) = 1.45nm**
- **Very high NMOS Idsat**
  - **Idsat = 1.66mA/um, Ioff = 37nA/um at Vcc = 1.3V**
- **Very high PMOS Idsat**
  - **Idsat = 0.69mA/um, Ioff = 25nA/um at Vcc = 1.3V**

# High-K/Metal-Gate NMOS $I_{on}$- $I_{off}$



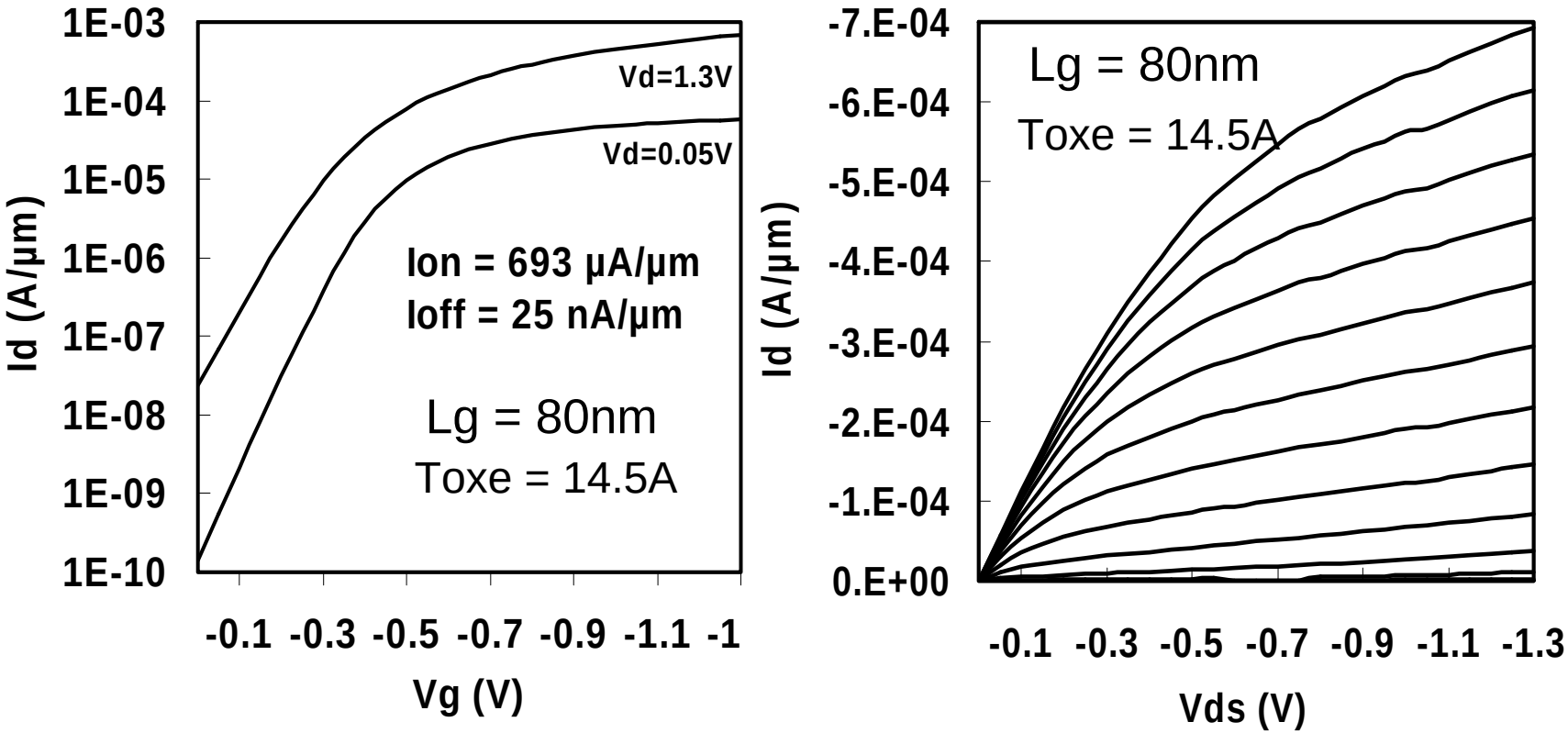
# High-K/Metal-Gate NMOS with Record-Setting Drive Current Performance




- **Electrical Tox at Inversion (Toxe) = 1.45nm**
- **Transistor physical gate length (Lg) = 80nm**

# High-K/Metal-Gate PMOS with Record-Setting Drive Current Performance




- **Electrical Tox at Inversion (Toxe) = 1.45nm**
- **Transistor physical gate length (Lg) = 80nm**

# Summary

- **We have implemented 1.2nm physical SiO2 in our 90nm logic technology node and products, and have demonstrated 0.8nm physical SiO2**
- **We have engineered and demonstrated NMOS and PMOS high-K/metal-gate stacks on bulk Si with i) the correct work functions, ii) channel mobility close to SiO2's and iii) very low gate leakage**
- **We have fabricated high-K/metal-gate NMOS and PMOS transistors on bulk Si with record-setting drive current performance**
- **We believe high-K/metal-gate is an option for the 45nm logic technology node, to be in production in 2007**