Advanced Depleted-Substrate Transistors: Single-gate, Double-gate and Tri-gate (Invited Paper)

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1. Introduction

It has been shown that the use of fully-depleted SOI transistors improves subthreshold slope and reduces DIBL. Fully-depleted SOI comes in the form of a single-gate depleted-substrate transistor (DST) [1], as shown in Figure 1a, or in the form of a double-gate transistor such as FinFET [2], as shown in Figure 1b. One of the main challenges of scaling the fully-depleted SOI transistors is the scaling of silicon body dimensions with reducing transistor gate length. In the case of single-gate DST, in order to maintain full substrate depletion, the silicon body thickness (T_{Si}) needs to be about 1/3 of the gate length (Lg) [1]. In the case of double-gate devices, since each gate controls half the body thickness, T_{Si} is equal to two-thirds of Lg [2].

Figure 2 shows the silicon body thickness (T_{Si}) requirement needed to provide full substrate depletion with respect to transistor gate length for both the single-gate DST and double-gate FinFET. It can be seen that for a given transistor gate length, the silicon body thickness requirement of the double-gate transistor is less stringent compared to that of the single-gate DST. However, the double-gate transistor requires printing the fin width (T_{Si}) 30% smaller than the transistor gate length (Lg). This makes the double-gate transistor not practical to fabricate since the most critical lithography step in fabricating the double-gate transistor is no longer the transistor gate patterning, but the fin patterning.

A tri-gate depleted-substrate transistor, on the other hand, can be used to overcome the silicon thickness shortcoming. In the case of the tri-gate DST, T_{Si} is equal to Lg in order to achieve full substrate depletion, as shown in Figure 2. Of the three fully-depleted SOI transistor structures discussed, tri-gate DST has the least stringent T_{Si} requirement. In addition, it is more practical than the double-gate transistor because both the transistor gate length and the fin width are equal and printed with the same lithography technology.

2. Tri-Gate Depleted –Substrate Transistor (DST)

Figure 3 shows the structure of a tri-gate DST. The tri-gate structure resembles the double-gate structure except it has an additional top gate electrode. Compared to the double-gate transistor, the tri-gate DST has shorter silicon fin height and wider silicon fin width. Each gate of the tri-gate device controls a portion of the silicon surface, as shown in Figure 3. To ensure full substrate depletion, the whole silicon body needs be depleted, and this can be done by varying the height and width (T_{Si}) of the silicon fin (silicon body) simultaneously. Fig. 4 shows the modeled silicon width and height requirements for full substrate depletion for tri-gate devices with 60nm and 30nm Lg. For very large silicon width, the tri-gate device is single-gate DST-like, and for very tall silicon height, the tri-gate device is double-gate transistor-like. An optimal tri-gate DST will have device dimensions of gate length = silicon body width = silicon body height.

3. Subthreshold slope and DIBL of Tri-gate DST

Figure 5 shows a cross section of the silicon body (fin) of the tri-gate transistor with Lg = 60nm. In this example, the silicon fin width (T_{Si}) is ~70nm. The silicon body height is ~40nm, over twice that needed for single-gate DST's. Figures 6 & 7 shows the Id-Vg and Id-Vd curves respectively of the n-MOS tri-gate device. The device show excellent sub-threshold slope of 69mV/decade and DIBL of 41mV/V at Vcc = 1.3V, indicating full depletion. The p-MOS (Figures 8 & 9) also shows excellent characteristics, with a sub-threshold slope of 71 mV/decade, and DIBL of 52mV/V at Vcc = 1.3V

4. Conclusion

All the three fully-depleted SOI transistor structures discussed (single-gate, double-gate and tri-gate) can achieve excellent subthreshold slope and DIBL characteristics. Of the three, the tri-gate depleted substrate transistor has the least stringent silicon thickness and silicon width requirements.

5. References

[1] R.Chau et al., IEDM Tech. Digest, pp. 621-624, 2001.

[2] N. Lindert et al, IEEE El. Dev. Lett., **22**., pp.487 –489, 2001.

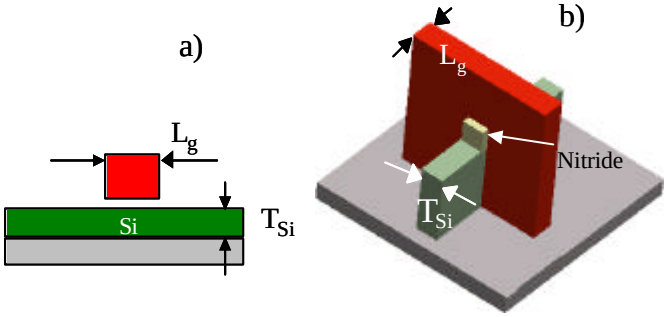

Figure 1. Single-gate (a) and double-gate (b) DST transistors showing L_g and T_{si} in each case

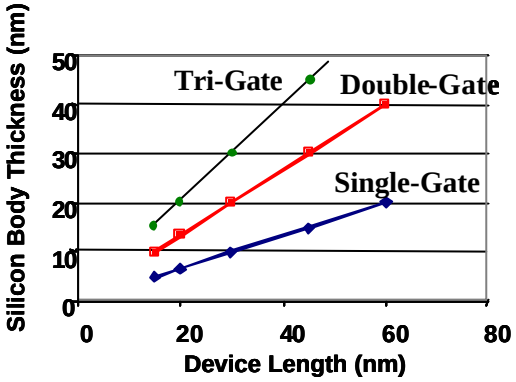

Figure 2. Thickness requirements for the silicon body of Single-Gate DST (diamonds), Double-gate DST's (squares) and Tri-gate DST's (circles)

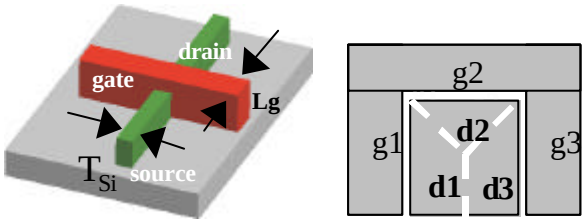

Figure 3. Representation of Tri-gate structure, with cross-section of the gate/channel region

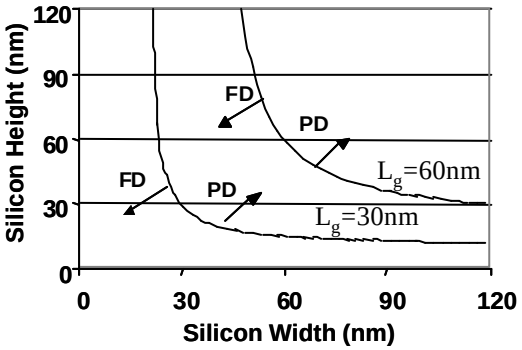

Figure 4. Silicon body height and width conditions for fully depleted (FD) and partially depleted (PD) substrates of Tri-Gate devices

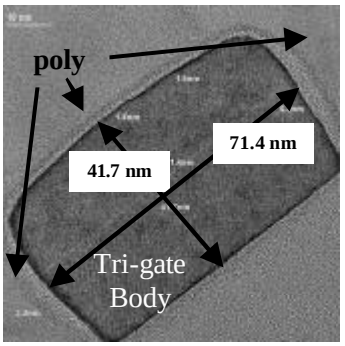

Figure 5. TEM of the silicon body of a Tri-gate device with height 41.7nm and width of 71.4nm

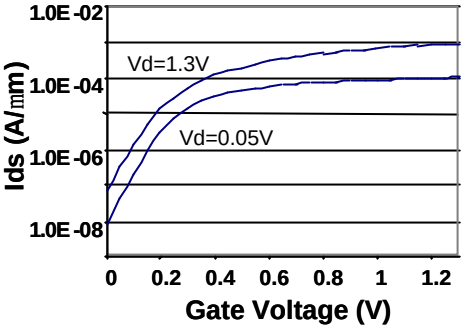

Figure 6. Id-Vg characteristics of a 60nm n-MOS Trigate device

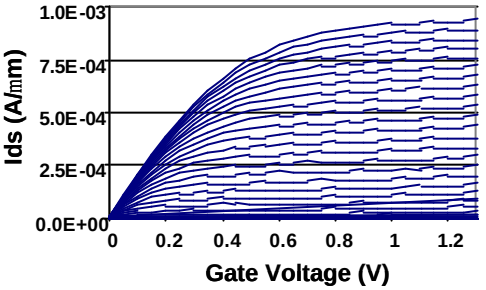

Figure 7. Id-Vd characteristics of a 60nm n-MOS Trigate device

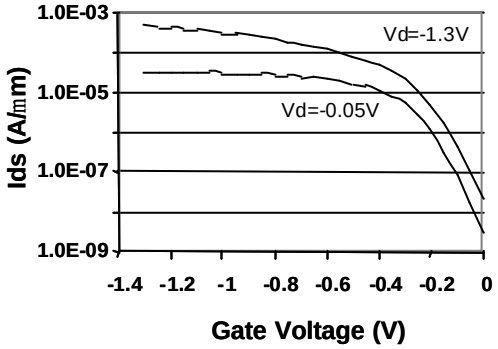

Figure 8. Id-Vg characteristics of a 60nm p-MOS Trigate device

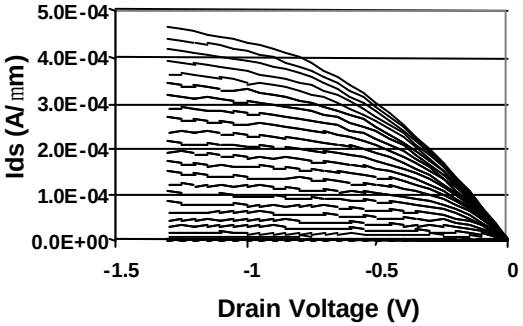

Figure 9. Id-Vd characteristics of a 60nm p-MOS Trigate device