

Chemicals and Gases in the Decade of Materials for the Semiconductor Industry

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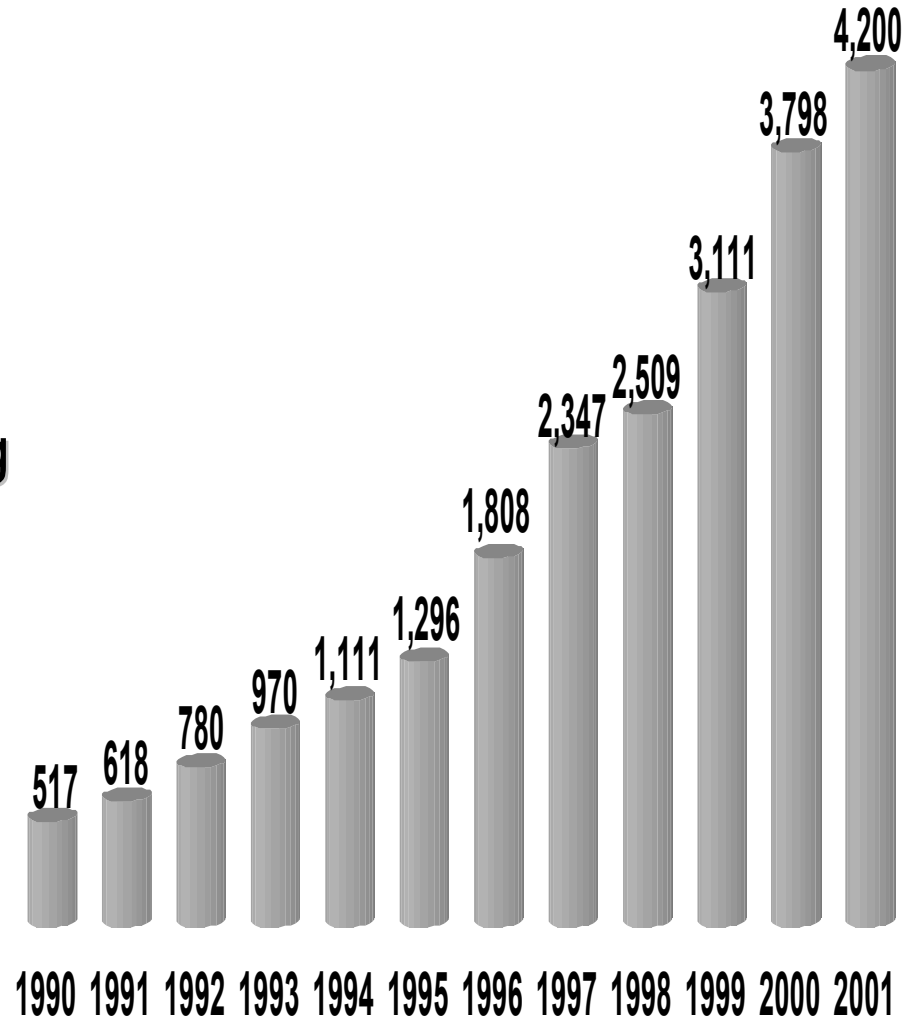
Our Business Environment

- **Increasing Global development & manufacturing**
- **Downward price pressure**
- **Increasing chip manufacturing complexity**
- **Increasing environmental regulations**

Intel Response: Invest for Innovation

World's first 300 mm silicon research lab

- Dedicated space for our most advanced and/or speculative silicon technologies
- 115K sq ft research building
 - ~ 56K sq ft of class 1 clean room at build-out
 - 28K sq ft in phase 1
 - Clean room link to development fabs



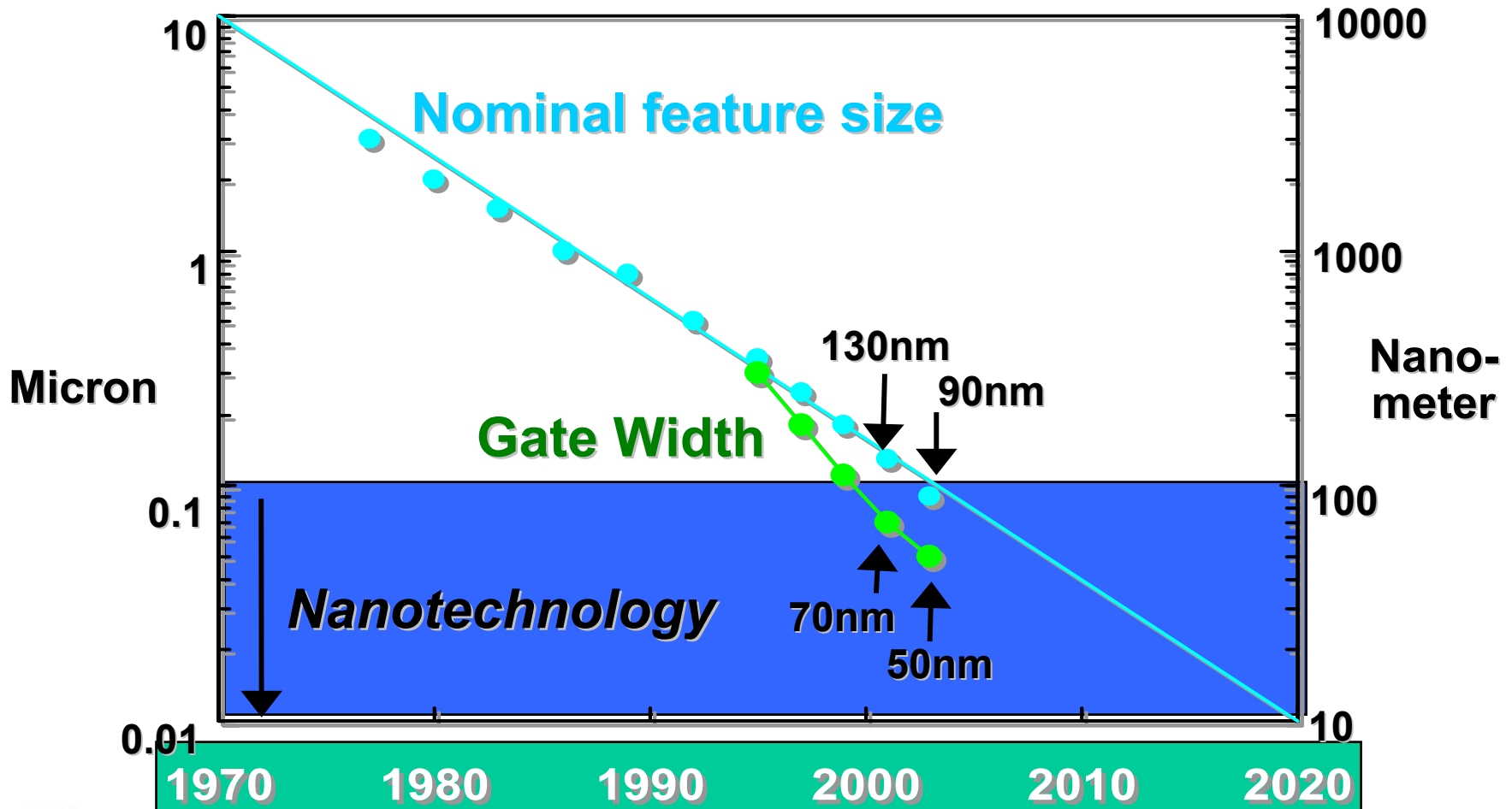
Intel Response: Innovate per Moore's Law

Process Name	<u>P856</u>	<u>P858</u>	<u>Px60</u>	<u>P1262</u>	<u>P1264</u>	<u>P1266</u>	<u>P1268</u>
1 st Production	1997	1999	2001	2003	2005	2007	2009
Lithography	.25μm	.18μm	.13μm	90nm	65nm	45nm	32nm
Gate Length	.20μm	.13μm	<70nm	<50nm	<35nm	<25nm	<18nm
Wafer Size (mm)	200	200	200/300	300	300	300	300
	Manufacturing			Development		Research	

“New technology generation every 2 years”

- **2x die per wafer**
- **1/2 transistor cost**
- **2x microprocessor speed**

Intel Response: Embrace the age of nanotechnology



What is Nanotechnology

- **Structures measured in nanometers**
 - **Less than 0.1-micron (100nm)**
- **New materials and device structures**
 - **Incrementally changing silicon technology base**
- **Materials manipulated on atomic scale**
 - **In one or more dimensions**
- **Increasing use of self-assembly**
 - **Using chemical properties to form structures**

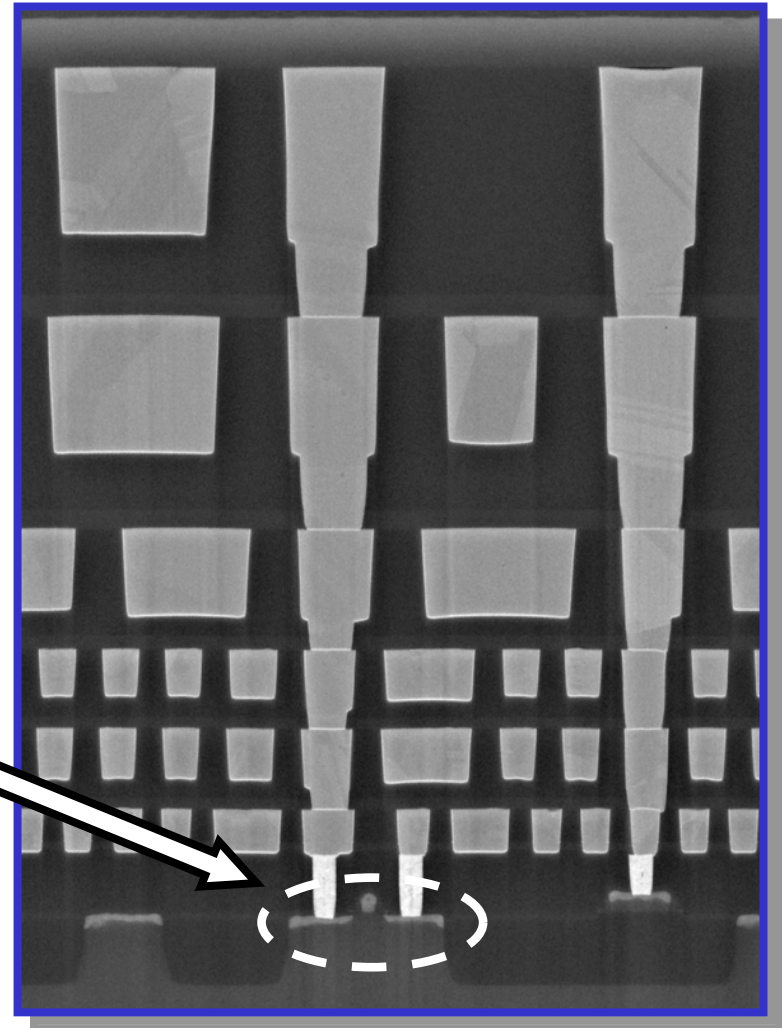
Intel's Innovation Challenge's

Interconnect

- Low K Dielectric
- Resist Removal on Low K
- Improved EM and Resistivity

Transistors

- High K Dielectric
- Novel "Silicon"
- Print smaller Dimensions

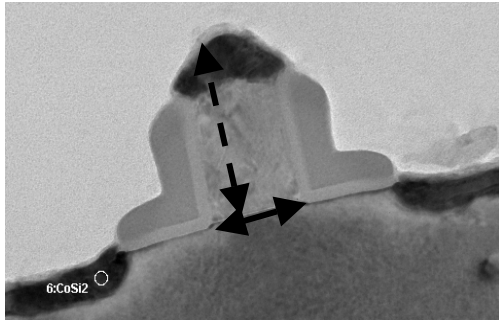


Intel Transistor Innovation

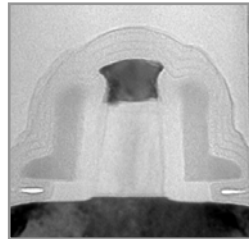
Industry-leading transistor performance on Intel's 90 nm process :

- 1.2 nm gate oxide Industry Thinnest
- Strained silicon Industry first HVM

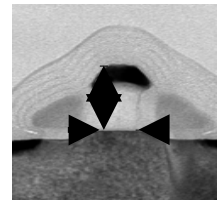
130nm Node



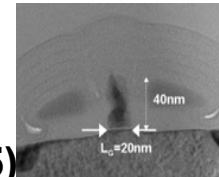
90nm Node



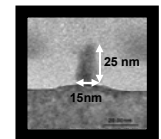
65nm Node



45nm Node



32nm Node



Strained Silicon

Terahertz

Tri-gate

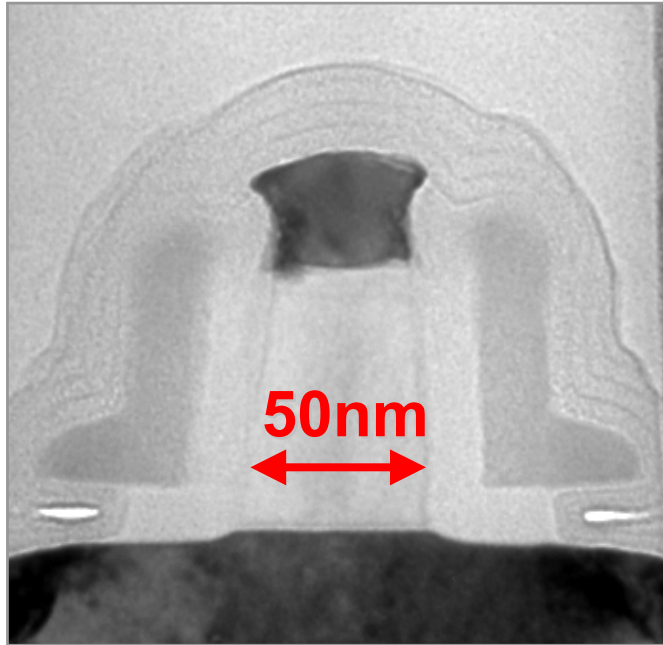
50nm Length
(Production in 2003)

30nm Prototype
(Production in 2005)

20nm Prototype
(Production in 2007)

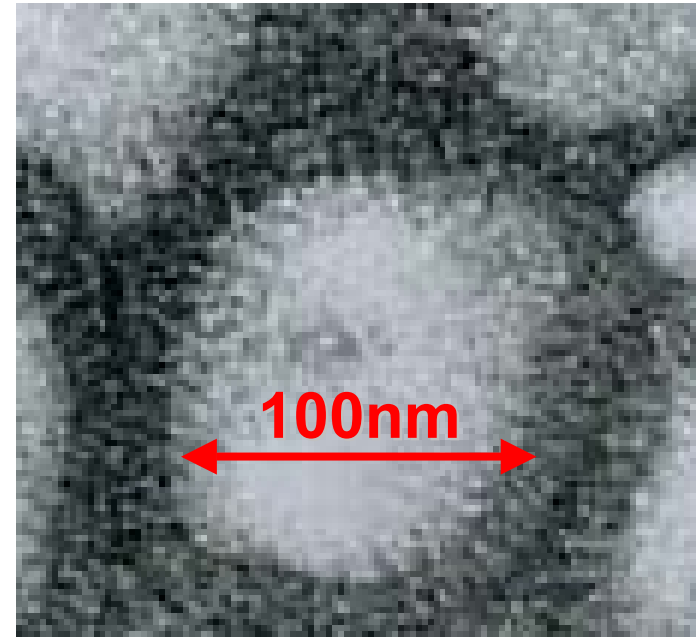
15nm Prototype
(Production in 2009)

Transistor Scaling Perspective



**Transistor for
90nm process**

Source: Intel



Influenza virus

Source: CDC

New Materials, Devices Extend Si Scaling

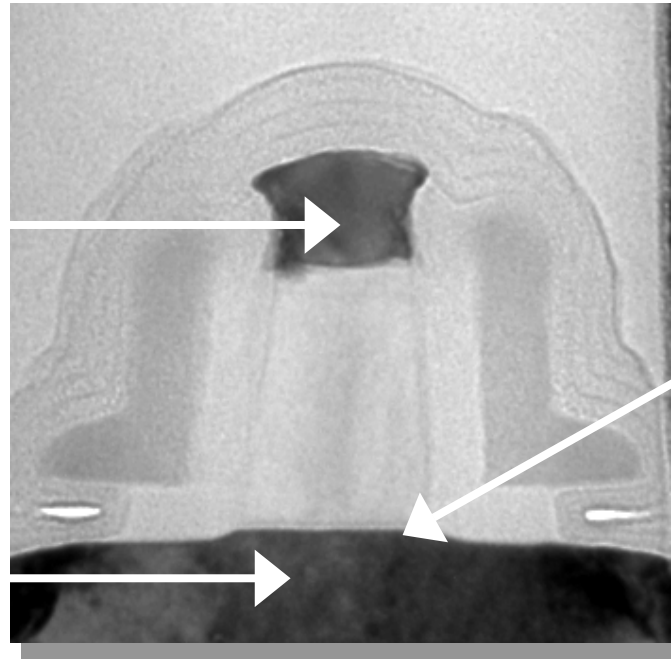
Changes Made

Gate

Silicide added

Channel

Strained silicon



Future Options

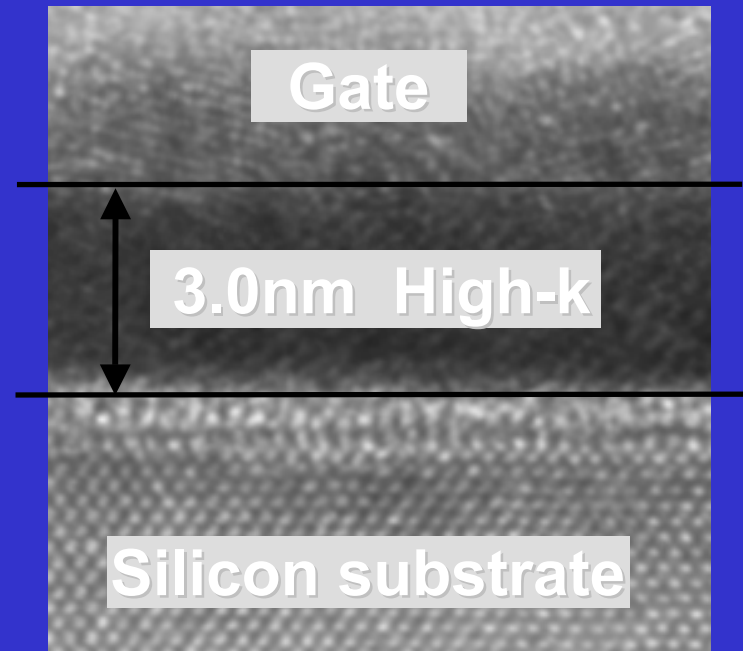
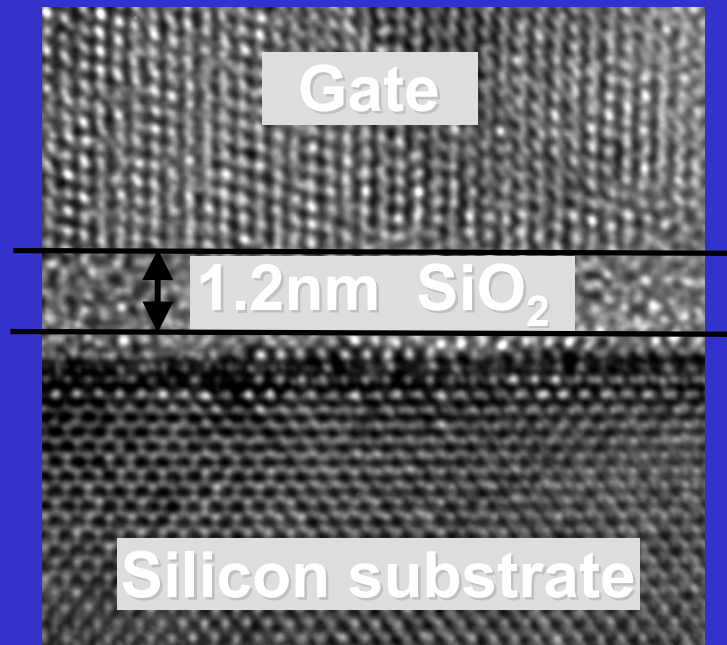
High-k gate dielectric

New transistor structure

Transistor

Source: Intel

Nanotechnology for Gate Dielectrics



Source: Intel

90nm process

Experimental high-k

Capacitance

1X

1.6X

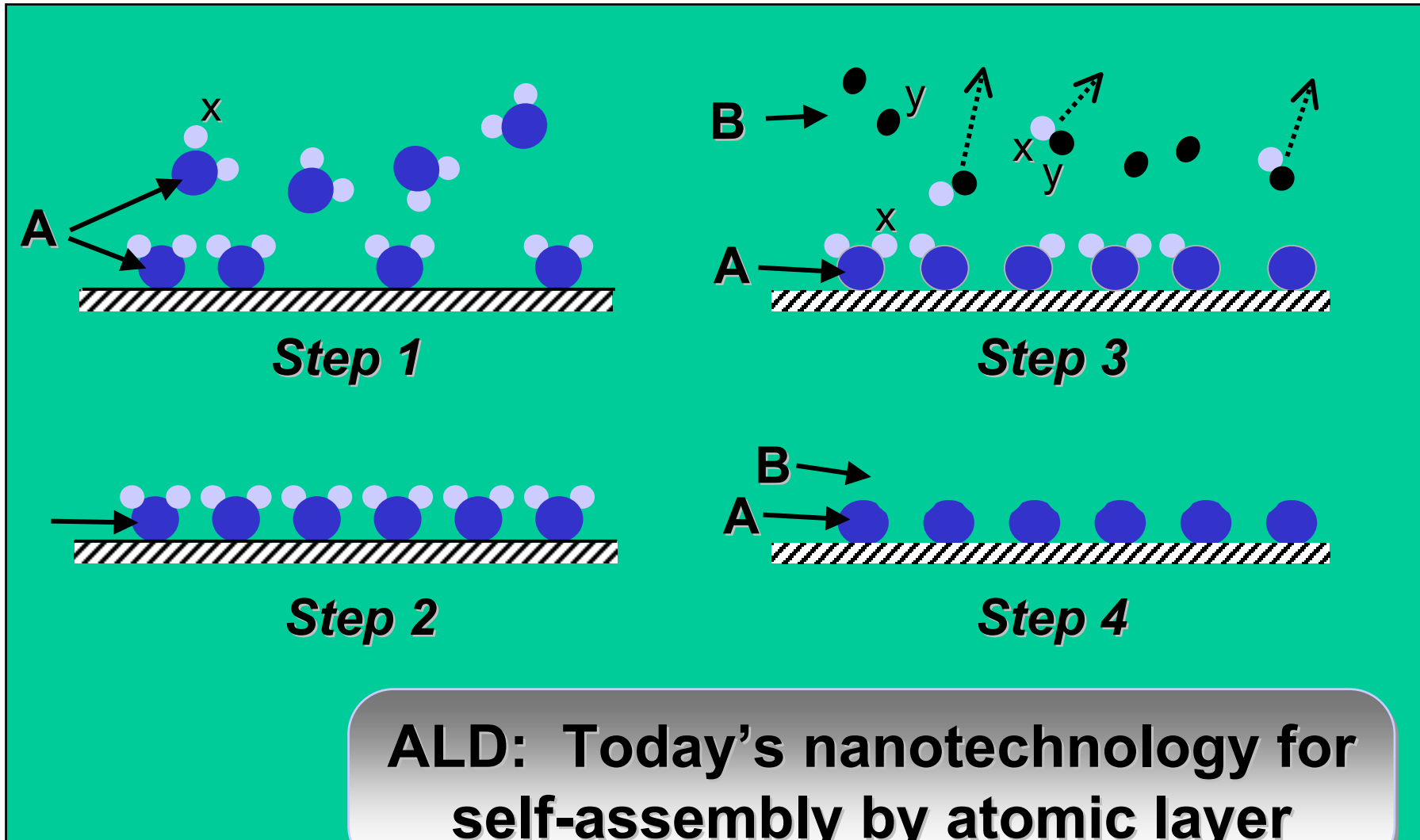
Leakage

1X

< 0.01X

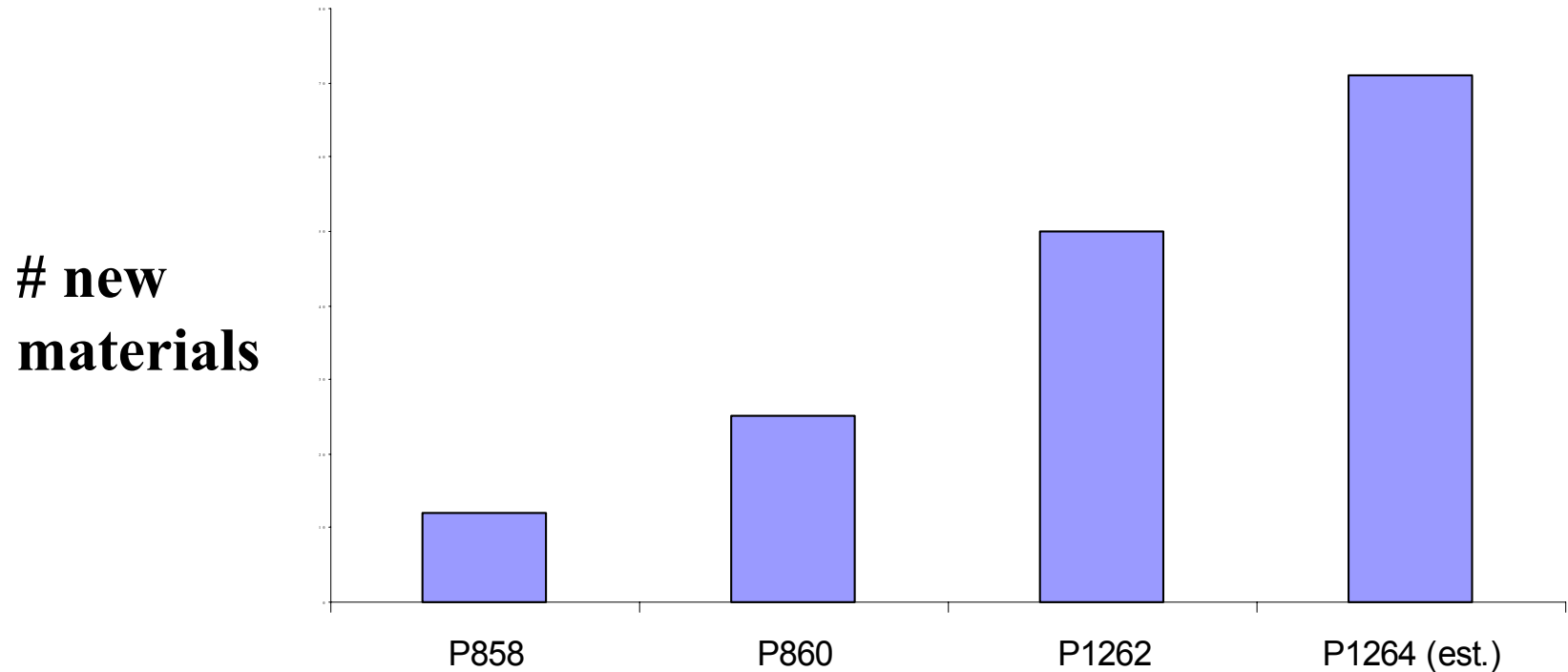
Integration is the key challenge

Crafting Films with Atomic Layer Deposition



ALD: Today's nanotechnology for self-assembly by atomic layer

Nanotechnology Decade is the Materials Decade



Specialty materials evaluated

–2001 hundreds of materials

–2003 thousands of materials

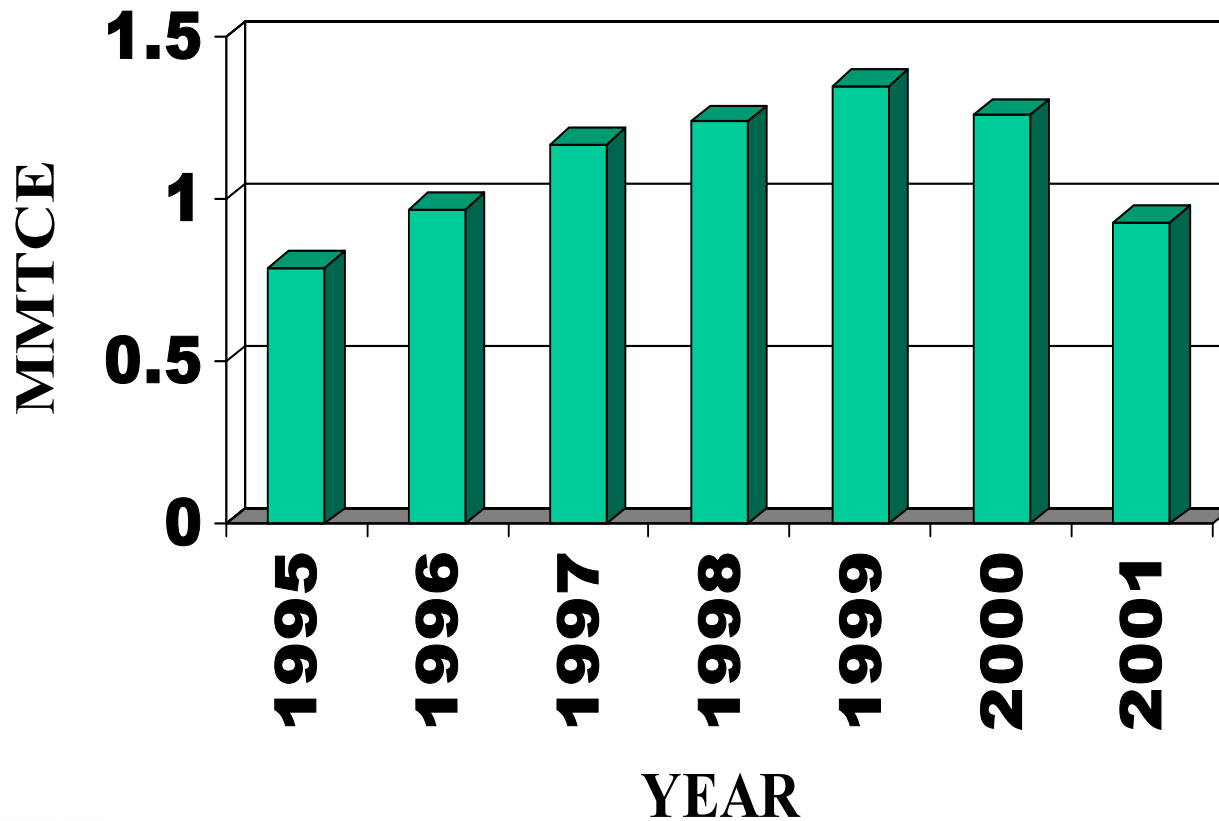
Chem & Gas Solutions Must

- Meet performance requirements
- Consistently deliver Statistically equivalent product
- Have a Secure Global Supply
- Deliver Global Service
- Pricing consistent with end product model
- Be Safe & be recognized safe
- Be Green and be recognized green

Support Request

- **Utilize Chem & Gas industry core competency to enable our success**
- **Closer collaboration --- many solutions will be dependent on our “architecture”**
- **Proactive management of the myriad of Environmental legislation and concerns everywhere.**

SIA Partners PFC Emissions



EU CHEMICALS PROGRAM

- **EU implementing a broad new regulatory system which proposes major restrictions to using new and existing chemicals**
 - **No unacceptable risk during life cycle - determined before chemical is introduced (or continues) in use – requires third party review**
 - **Chemicals of “high concern” subject to public disclosure**

IMPLICATIONS

- **Geographical disparity in use versus global scope creep**
- **Time to authorization delays estimate of 6-12 months compared to non-EU programs**
 - Increase cost of chemicals and gases
 - Innovation rate different in EU vs ROW
- **“Green” lists (between 1-7) would impact some (or many) new and existing process chemicals**
- **I.P. on new and novel materials may be jeopardized**

Further discussion Opportunity: 7:00 PM Terrace Room