Purpose of Work

• Get off CPU functional testing / tester treadmill
• Optimize product - content - testers for cost
• Risk manage test quality during migration
Outline

• Timeline Overview
• 1st and 2nd Generation Structural Testers
  – Architectural Choices
  – Expected Test Content and Flow
• Data from Pentium® 4 Processor
• Future Trends
Migration is a Process, not an event

1993
Partitioned Strategy defined

1995
1st gen ST defined
1st gen ST delivered

1997
2nd gen ST defined
2nd gen ST delivered

1999
Distributed Test Strategy defined
Pentium® 4 Processor DFT defined
1st Pentium® 4 Processor production

2001
Definition of 1st Gen Struc Tester

• Key Goals
  – Get off treadmill for higher speed testers
  – Achieve lower cost by reduced capability
    Plan for ST to run only scan + memory tests
  – Enable parallel testing

• Consider but rejected
  – Adding scan to FT — still on treadmill
  – Eliminate FT entirely — test quality risk
Architectural Choices for ST

- Test Pattern Generator
- Timing and Format
- Pin Electronics
- Device Interface
- Test Controller
- Power Supplies

Memory Depth, Speed
Speed, Flexibility, Accuracy
Bandwidth

Accuracy, Speed, Capacity
Architectural Choices

- Test Pattern Generator
- Timing and Format
- Unidirectional
  - Lower speed
  - Reduced width
- Power Supplies
- Test Controller
- Device

Cut width & freq

- 200+ ⇒ 128 pins
- 400 ⇒ 200 MT/S
- ~4x cost savings
## Testability Port

<table>
<thead>
<tr>
<th>Function</th>
<th>Capability</th>
<th>Pin Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scan inputs</td>
<td>200 MT/S, 1nS</td>
<td>36-48</td>
</tr>
<tr>
<td>DUT outputs</td>
<td>200MT/S, &quot;</td>
<td>36-48</td>
</tr>
<tr>
<td>Array address</td>
<td>200MT/S, &quot;</td>
<td>Up to 36</td>
</tr>
<tr>
<td>Array data inputs</td>
<td>200MT/S, &quot;</td>
<td>Up to 36</td>
</tr>
<tr>
<td>Control &amp; JTAG</td>
<td>200MT/S, &quot;</td>
<td>24</td>
</tr>
<tr>
<td>Clocks</td>
<td>200MHz, 300pS</td>
<td>Up to 4</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>128-152</strong></td>
</tr>
</tbody>
</table>

Compatibility Enforced at Product Design
Architectural Choices

- Test Pattern Generator
- Test Controller
- Power Supplies

Unidirectional
- Lower speed
- Reduced width

Timing and Format

Reduce time sets and formats

16 dynamic time sets ⇒ single 3bit scan model
Architectural Choices

- Broadside
  - Memory Pattern
  - Scan Pattern
  - Capture
  - Source Select

- Timing and Format
- Unidirectional
- Lower speed
- Reduced width

Replace large broadside mem with deep scan

Test Controller

Power Supplies

Device

128Mbit scan (shared)
32M ⇒ 4M broadside
Definition of 1st Gen Struc Tester

• Key Goals
  – Get off treadmill for higher speed testers
  – Achieve lower cost by reduced capability
    Plan for ST to run only scan + memory tests
  – Enable parallel testing

• Key Definition Features
  – 128 pin testability port
  – N-1 generation tester interface speed
  – Deep and shared scan memory
  – APG running at full interface speed (see paper)
Evolving Outlook for Content

OLD VIEW  Partitioned testing (Early 90’s)
  • Scan + memory testing on structural tester
  • Full chip vectors on functional tester

NEW VIEW  Distributed Test (1997+)
  • More and varied defect types to detect
  • Multiple content types on multiple platforms
    Functional on Func, Structural on Struc
    + Func content on structural tester
    + Struc content on functional tester
Defect Spectrum

- Defect Based Self-Test on Structural Tester
- Defect Based Off-chip on Structural Tester
- Functional Self-Test on either ST or FT
- Full chip vectors on Functional Tester
Distributed Test Platforms

Wafer Test → Package Test

- Structural Sort
  - 128pin, 200MT/s
  - Tight T/V/F control
  - Cover hard defects

- Burn-In
  - 4pin, 75 MT/s
  - Loose T/V/F control
  - Time intensive tests

- Structural Class
  - 128pin, 200MT/s
  - Tight T/V/F control
  - Cover hard defects
  - Hard + Soft defects
  - Some speed tests

- Functional Class
  - Full pin, full spd
  - Tight T/V/F control
  - Soft defects + speed
  - Minimize test time

Define partitioning based on economics, not capability.
Segmentation enables FT reuse.
New Architectural Choices for ST2

• Increase flexibility for mixed content
  – Large Vector Mem increase to 16M
  – Parameter passing to SVM
  – Bidirectional pins
  – 1GBit scan memory depth

• Move pin drivers to mainframe
  – Not needed for interface speed
  – Higher level of board integration
  – Test head contains only power supplies

• Outcome
  – 2x reduction in space
  – >2x improved MTBF
  – Further 2x cost reduction
Pentium® 4 Processor
Production Data

• Multiple content types on multiple platforms
  – Legacy full chip functional vectors on FT
  – New internal functional tests on ST
  – Scan tests on ST
  – Array testing, APG and BIST, on ST
  – Defect based I/O tests on ST or FT
  – Special purpose tests on ST or FT
  – Both ST1 and ST2 are in production
Partitioning by Test Type by Time

- **Param**
- **I/O**
- **Logic**
- **Cache**
- **Misc**

**Entirely on Struc Tester**

**Split btw Func & Struc Tester**

**Wafer test – 100% on ST**

**Package test – 77% on ST**
Key Achievements

• Achieved ST migration including speed tests
  – Fallout tracks content, not platform
  – Logic-cache internal speed paths on ST
  – Other full chip speed paths on FT
  – Parallel test enabled

• Achieved key cost goals
  – 2002 CPU has 18x more xtors than 1995
  – Test cost per unit is lower than 1995
  – Intel tester capital greatly reduced
  – Per site tester cost 1/10 of functional tester
Prior to 1997, Intel test capital followed ISTR Trend
Today our test capital is scaling with Si trends
Moore’s Law to Continue

Transistor counts increasing to meet demand for performance and functionality
Test must keep up the pace!

>1B transistor CPU on your desk by 2010
>12 Mbytes Cache
>60M Logic Gates

2X growth in 1.96 years!
Future Trends
(or how to test a billion transistors)

• Cache content growing
  – Test time
  – Yield / redundancy
  – Stability tests
  – New memory types

• Logic complexity
  – High GHz
  – Shallow logic
  – Soft Errors
  – New transistors and materials

Mobile Pentium® III Processor
Test Times Endanger Product Cost

- Data Volume increasing beyond tester limits with addition of multiple fault models
- Real problem is test time and affordability
  - Need improved bandwidth, data density, or much cheaper platforms
Possible Tester Directions

Wafer Test → Package Test

Structural Sort → Burn-In

Struc Class

Func Class

Alternative A
- Develop ST3
  - Site cost 2-4x less
  - More parallel sites
  - Or cheaper platform

Alternative B
- Enhance ST platform
  - More capable
  - Same price
- Eliminate FT step
Functional Tester Elimination

- Currently 77% converted to ST platform
- Of remaining 23%
  - 1/2 of failing patterns have low bus activity
  - 3/4 of down bin patterns have low bus act.
  - Potential moveable
- ST enhancement
  - Generate subset of full chip patterns
  - Swappable bus specific interface
Conclusions

• Optimize product - content - testers together
• Choose right content to test the defects
• Be flexible to allow for changing test needs

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