High Performance Non-Planar Tri-gate Transistor Architecture

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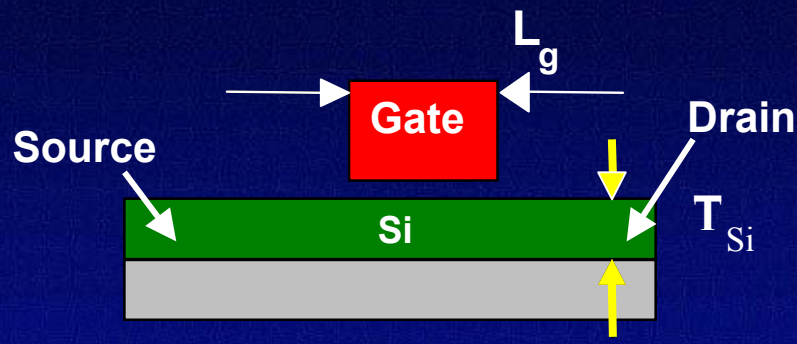
What Are We Announcing?

- Previously we disclosed the invention of a novel experimental non-planar Tri-gate transistor structure (Sept 17, 2002 at ISSDM, Nagoya Japan)
- Since then, improvements have been made and the tri-gate transistor continues to show higher performance and better scalability than conventional bulk Si transistor
- 60nm tri-gate transistor achieves world-record non-planar NMOS performance and low leakage*
- Scalability to 30nm gate length has also been demonstrated
- These tri-gate transistors were fabricated in D1C, which is our 300mm development and manufacturing Fab in Oregon for the 90nm process generation
  - Tri-gate basic process steps are similar to the current baseline manufacturing process
- Tri-gate transistor has gone beyond the research phase and is now entering the development phase
- Tri-gate transistor allows Moore's Law to continue and is one of the key transistor options being evaluated for Intel's 45nm process generation (2007 production)

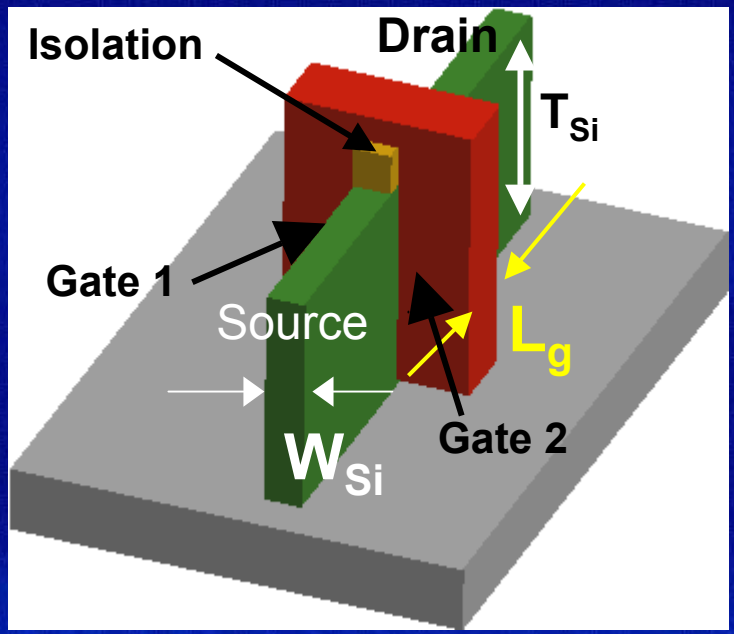
Intel

* I_{Dsat} = 1.23mA/um and Ioff = 40nA/um at Vcc = 1.3V

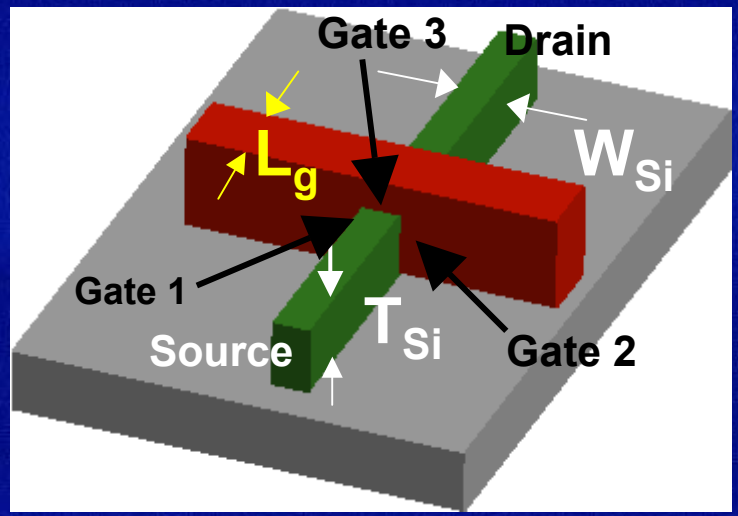
Transistor Architectures



(Planar)



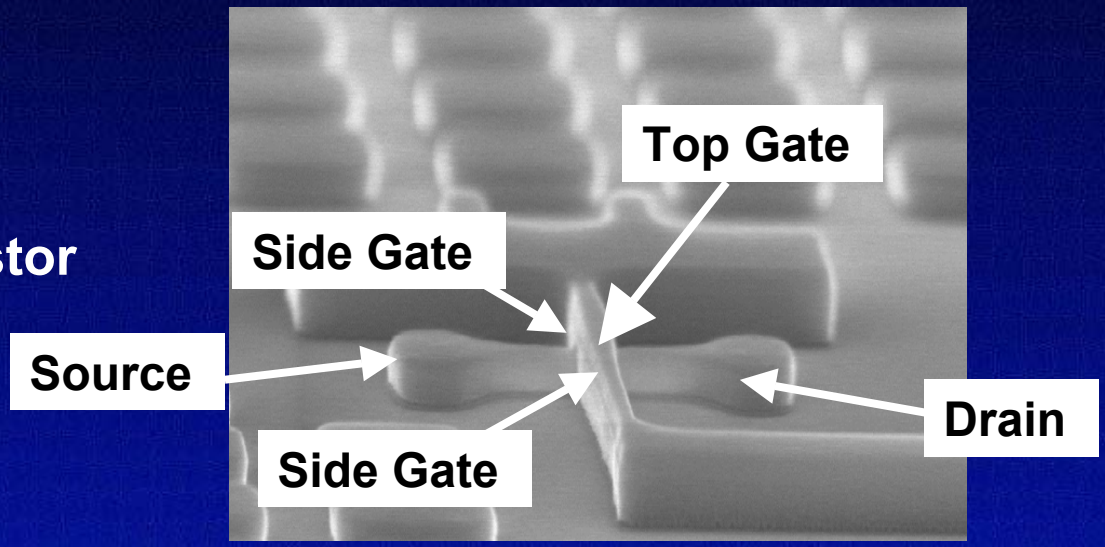
Double-gate (e.g. FINFET)
(Non-Planar)



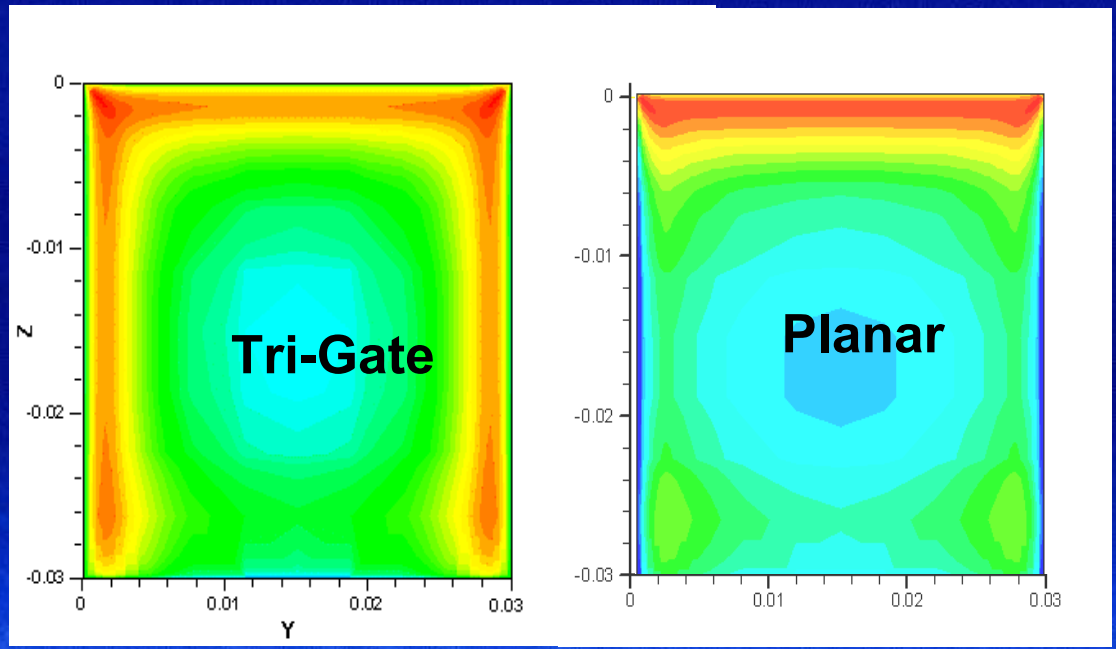
Tri-gate
(Non-Planar)

Tri-gate Transistor

Actual photo
30nm Tri-gate transistor

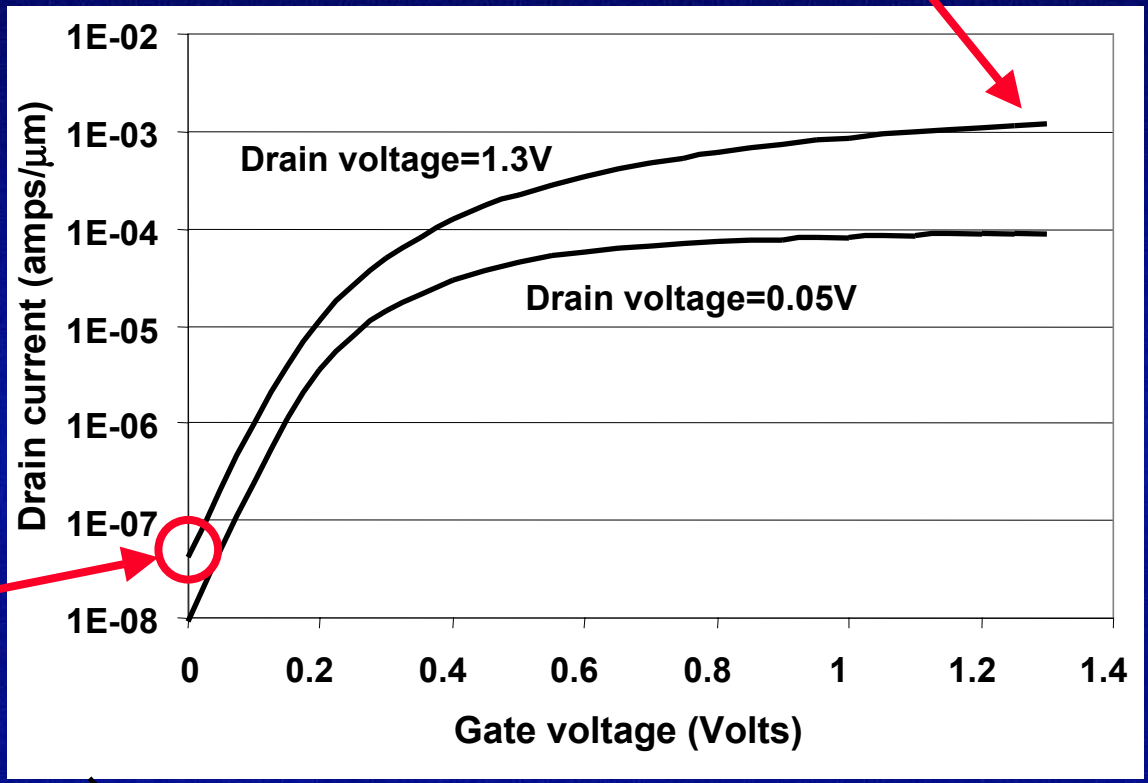


Simulation
Cross-section of silicon channel shows much more current flow (indicated by red) in tri-gate transistor than in planar transistor



World Record Non-Planar Performance

Very high drive current at saturation, 1.23 mA/μm



Very low leakage, 40nA/μm

Tri-gate transistor exhibits excellent device characteristics

Additional details of the Tri-gate transistor design and technology will be presented at the 2003 Symposium on VLSI Technology in Kyoto Japan on June 12, 2003

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon